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## Topical Review

# Novel fabrication techniques for ultra-thin silicon based flexible electronics

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**Abstract**

Flexible electronics offer a multitude of advantages, such as flexibility, lightweight property, portability, and high durability. These unique properties allow for seamless applications to curved and soft surfaces, leading to extensive utilization across a wide range of fields in consumer electronics. These applications, for example, span integrated circuits, solar cells, batteries, wearable devices, bio-implants, soft robotics, and biomimetic applications. Recently, flexible electronic devices have been developed using a variety of materials such as organic, carbon-based, and inorganic semiconducting materials. Silicon (Si) owing to its mature fabrication process, excellent electrical, optical, thermal properties, and cost efficiency, remains a compelling material choice for flexible electronics. Consequently, the research on ultra-thin Si in the context of flexible electronics is studied rigorously nowadays. The thinning of Si is crucially important for flexible electronics as it reduces its bending stiffness and the resultant bending strain, thereby enhancing flexibility while preserving its exceptional properties. This review provides a comprehensive overview of the recent efforts in the fabrication techniques for forming ultra-thin Si using top-down and bottom-up approaches and explores their utilization in flexible electronics and their applications.

Keywords: flexible electronics, silicon fabrication technique, top-down approach, bottom-up approach

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## 1. Introduction

The emergence of flexible electronics has significantly broadened their application areas beyond what conventional rigid-based electronics can achieve [1–5]. This expansion is driven by the advantages of flexibility, lightweight design, portability, and high durability [6, 7]. These advantages that provide excellent conformal contact with having low Young's modulus enhance their capability to adapt to highly curved environments, ensuring prolonged measurement accuracy and enhanced electronic stability.

Table 1 presents the properties of semiconducting materials classified into organic, carbon-based, and inorganic materials as possible candidates for flexible electronics. This table introduces key material properties relevant to their use in electronics. Organic materials, including conducting polymers [8, 9] and organic–inorganic hybrid materials [10–13], are intrinsically soft and flexible [14, 15]. They benefit from low temperature solution processes, making them suitable for flexible substrates [16, 17]. Conducting polymers, in particular, offer excellent cost efficiency. However, they exhibit low electrical properties and durability because of their sensitivity to environmental factors such as temperature and humidity when compared to inorganic materials [14, 18, 19]. These properties limit the performance of the sensors and their compatibility with integrated circuit (IC) applications. On the other side, carbon-based materials, such as carbon nanotube and graphene, offer excellent electrical mobility due to their unique honeycomb-like crystal lattice structure and flexibility resulting from their two-dimensional nano-thin structure [20–22]. These properties make them well-suited for flexible electronics. Furthermore, their good reliability and compatibility with IC increase their utility. However, carbon-based materials pose challenges for practical use due to their poor cost efficiency [23–26].

Inorganic semiconducting materials which include III–V compounds [27, 28], metal oxides [29, 30], 2D materials [35–37], and silicon (Si) [31–34] are known for their overall high reliability and suitability for IC. Inorganic materials possess superior electrical properties but necessitate high-temperature processes [38, 39]. Additionally, they lack the flexibility due to their inherent stiffness, presenting challenges for their integration into flexible platforms [40]. Metal oxides have the advantage of low-temperature deposition processes, in contrast to typical inorganic materials. However, due to their unstable structural nature, metal oxide semiconducting materials exhibit low electrical mobility, limiting their utilization in various applications. Two-dimensional (2D) materials exhibit high overall properties, yet their cost efficiency is hindered by the expensive manufacturing processes. Furthermore, achieving high-quality, large-area 2D materials for industrial applications presents a challenge [41, 42]. In contrast, III–V compounds have excellent electrical mobility, but their low-cost efficiency, resulting from the high intrinsic material cost, and poor mechanical properties diminishes their practicality (table 1) [43, 44].

Among the wide variety of materials used in flexible electronics, Si remains the dominant material in electronics due to its mature fabrication process, decent electrical properties, reliability, and cost-effectiveness for various applications [31, 33, 45–47]. Si, as a semiconducting material, ensures a high level of production stability and reliability, which is why it remains the primary material choice for consumer electronics even to this day [48–50]. Moreover, in comparison to oxide semiconducting materials and organic semiconducting materials, which exhibit limited electrical mobility, Si has superior electrical mobility due to its diamond cubic and defect-free structure that provides smooth movement of electrons through the crystal lattice [51–54]. This advantage in mobility allows for faster switching speed, and higher drive current in transistor applications [55, 56]. Si also exhibits high scalability through a mature micro-fabrication process, employing nanoscale lithography to enhance channel density and ensure high yield [57–61]. These advancements have markedly elevated the maturity of Si-based electronics, facilitating the manufacturing of smaller, faster, and more efficient IC [62, 63]. Furthermore, the crystalline structure of Si provides it with exceptional thermal resistance and stable electrical performance, in contrast to organic semiconducting materials that often struggle with low thermal durability and poor electrical stability. This inherent stability ensures consistent and reliable functionality even under challenging conditions [64–66].

Based on cost efficiency, well-established manufacturing processes, high electrical mobility, scalability, and durability, Si finds extensive use in various flexible electronic applications [67, 68]. By adjusting doping levels, the conductivity of Si can be controlled, enabling it to serve as an insulator at low doping levels and a conductor at high doping levels [69, 70]. This adjustable conductivity makes Si the basis for electronic components, from basic electronics (e.g. transistor) to complex electronics (e.g. IC) [32, 71]. The well-known biocompatibility of Si not only paves the way to guarantee safety to the human body in bioelectronics [72, 73] but also enables conformal contact with the human body and organs through its low bending stiffness in a thin geometry (e.g. $<$a few hundred nanometers), enhancing the quality and performance of bioelectronics. Thus, the excellent biocompatibility and flexibility of Si make it for wearable [74–77], bio-implant [78–81], and biomimetic applications by using suitable structures and characteristics [82–84]. Furthermore, flexible Si electronics have led to advancements in the soft robotic field, improving stability, adaptability, and manipulation accuracy [85–87]. Beyond these applications, the advancements in reducing weight and increasing portability contribute to the development of the energy industries, encompassing flexible solar cells [88–90], batteries [91, 92], and energy harvesting devices (figure 1) [93, 94].

Si is categorized based on its crystalline phase and utilized according to its distinct properties [95–97]. Table 2 shows the key characteristics of single-crystalline Si, polycrystalline silicon (poly-Si), and amorphous silicon (a-Si). First,

**Table 1.** Organic semiconducting, carbon-based, and inorganic semiconducting materials properties.

| Material | Classification | Electrical mobility | Mechanical property | Cost efficiency | Reliability | IC compatibility | References |
|---|---|---|---|---|---|---|---|
| Organic semiconducting materials | Conducting polymer (PEDOT:PSS, PANI, PPy) | Poor | Good | Excellent | Poor | Poor | [8, 9] |
| | Organic–inorganic hybrid (Perovskite, MOFs) | Poor | Good | Poor | Poor | Poor | [10–13] |
| Carbon-based materials | CNT and graphene | Excellent | Excellent | Poor | Good | Good | [23–26] |
| Inorganic semiconducting materials | III-V compound (GaAs, GaN, InP) | Excellent | Poor | Poor | Excellent | Excellent | [27, 28] |
| | Metal-oxide (ZnO, IGO, IGZO) | Poor | Poor | Good | Good | Good | [29, 30] |
| | 2D materials (TMDs, TMDCs) | Good | Good | Poor | Good | Good | [29, 30] |
| | Bulk-silicon | Good | Poor | Good | Excellent | Excellent | [31, 32] |
| | Thin-silicon | Good | Good | Good | Excellent | Excellent | [33, 34] |

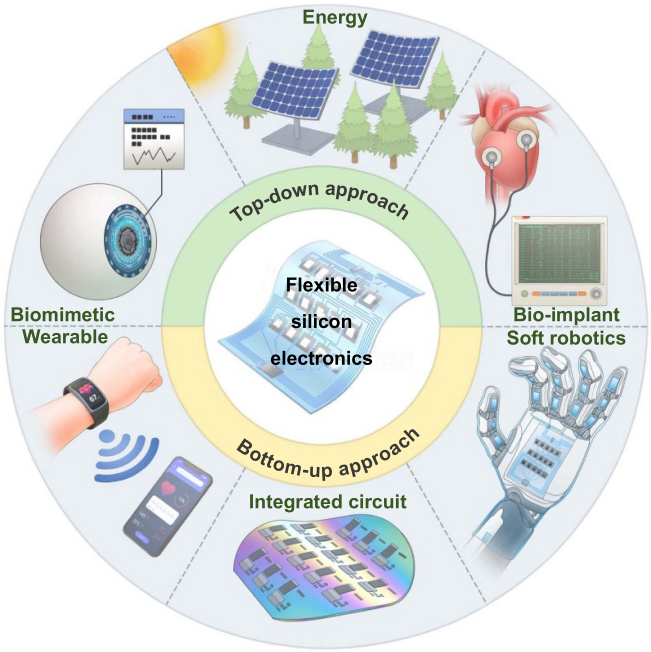


**Figure 1.** Applications of flexible silicon electronics: utilizing both top-down and bottom-up approaches in silicon fabrication.

single-crystalline Si has a nearly perfect diamond crystal lattice with almost no grain boundaries and defects. Due to the absence of defects, single-crystalline Si exhibits higher Young's modulus (e.g. 130–188 Pa) and density compared to poly-Si and a-Si [98–103]. Furthermore, owing to its crystal structure with a defect-free lattice and low scattering that enables easier movement of electrons, it exhibits an impressive electron mobility of up to 1400 $cm^2 \cdot V^{-1} \cdot s^{-1}$, leading to a rapid processing speed that makes it ideal for high-performance IC like microprocessors and memory chips [51–54]. However, single-crystalline Si is challenging to be used in flexible Si electronics directly owing to its high processing temperature, approximately 1415 °C [104]. Second, poly-Si exhibits a unique micro-structure in which individual crystal grains are randomly arranged, leading to the presence of characteristics such as grain boundaries and defects. This structure results in a higher thermal expansion, making it advantageous for thermal sensor applications [105]. However, due to the defect structure that hinders electron movement, poly-Si has lower electron mobility compared to single-crystalline Si. Despite this drawback, poly-Si has attracted attention in the display industry because of its cost efficiency compared to single-crystalline Si, combined with the advancements in low-temperature polycrystalline silicon (LTPS) technology. LTPS is the process of converting a-Si into poly-Si at temperatures below 450 °C, which is lower than that required for processing single-crystalline Si [106–108]. Finally, a-Si is formed by a continuous random network of disordered Si atoms lacking long-range order [109, 110]. This absence of a well-arranged lattice structure, along with defects such as grain boundaries and a density of states within the band gap, disrupts the movement of electrons, resulting in relatively lower electron mobility (Approx. 0.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$) compared to single-crystalline Si and poly-Si [111, 112]. Additionally, defects in a-Si fail to act as recombination centers, leading to a lack in the generation of electron–hole pairs crucial for electricity production. The lack of long-range order expands the bandgap, allowing for the absorption of a wider spectrum of light, especially in the visible range. This results in a more direct bandgap characteristic [95, 113]. With its unique optical properties, hydrogenated amorphous silicon (a-Si:H) is formed by introducing hydrogen atoms to compensate for the low performance of a-Si. When hydrogen atoms bond with a-Si, they attach to the dangling bonds present in a-Si, resulting in the formation of a-Si:H. This process reduces defect density and improves electron mobility, making a-Si:H suitable for various optoelectronic devices [95]. Furthermore, the processing temperature is below 250 °C, since a-Si is typically deposited through the chemical vapor deposition (CVD) process [114, 115].

**Table 2.** Properties of amorphous silicon (a-Si), polycrystalline silicon (poly-Si), and single-crystalline silicon.

| Property | Single-crystalline silicon | Polycrystalline silicon (poly-Si) | Amorphous silicon (a-Si) | References |
|---|---|---|---|---|
| Lattice structure | Perfect crystal lattice | Multiple small crystals and grains | Silicon atoms in a disordered arrangement | [95–97] |
| Young's modulus | 130–188 GPa | Variable based on grain size and orientation | Lower than crystalline forms | [98–101] |
| Density | 2.33 $g{\cdot}cm^{-3}$ | Similar to single-crystalline silicon | 1%–2% less than single-crystalline silicon | [102, 103] |
| Electron mobility | 1400 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ | 50–100 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ | Approx. 0.5 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ | [51–54] |
| Bandgap | Approx. 1.1 eV | Variable based on defect and grain size | Approx. 1.7 eV | [95, 113] |
| Processing temperature | Approx. 1415 °C | Below 450 °C | Below 250 °C | [104, 108, 116] |

Single-crystalline Si, poly-Si, and a-Si:H are distinguished by their crystal phases and find diverse applications based on their mobility characteristics. Single-crystalline Si, because of its defect-free structure and high electron mobility, serves as high-performance IC chips. In contrast, poly-Si, while offering lower electron mobility compared to single-crystalline Si, boasts cost efficiencies, used in the display industry where high performance is not required. A-Si:H exhibits enhanced electron mobility and wide band gap. Because of these advantages, a-Si:H efficiently absorbs light and can be used in optoelectronic devices such as solar cells. Additionally, its applications extend to touch-screen panels like e-books where high scanning rates are not critical [117, 118].

Conventional wafer-scale Si possesses high bending stiffness, which presents a challenge when integrating it into flexible electronics. Flexible electronics need to maintain their electrical performance while experiencing repetitive mechanical stress and strain such as bending or stretching [2, 7, 119]. To withstand such mechanical constraints, thinning Si has emerged as an essential solution. Reducing thickness results in a proportional decrease in both flexural rigidity and energy release rate (figures 2(a) and (b)) [33, 47]. This approach not only facilitates conformal applications to curved or dynamic surfaces but also accommodates non-planar geometries and multi-layer integration. Recent advancements have enhanced the durability and reliability of Si while reducing rigidity. These properties can be improved through the implementation of unique structural designs, such as serpentine or wavy structures (figure 2(c)) [120–124], and the protection of the device from external environmental factors and mechanical deformation through encapsulation methods [125–129]. Another challenge is the need to maintain low temperatures during the Si fabrication process in flexible electronics. The fabrication processes of Si electronics often involve high-temperature procedures such as high-quality doping or oxidation using the furnace. However, the materials often used as flexible substrates are typically polymer materials [130–132]. These materials have lower thermal stability compared to rigid substrates, which can lead to deformation, melting, or degradation, making them unsuitable for high-temperature processes [5, 51]. For this reason, flexible electronics employ either the deposition of Si at a low temperature or the transfer of a thin Si layer that has already been processed at a high temperature onto a flexible substrate [133, 134]. There are two main approaches for processing that both thin the Si and reduce the process temperature: top-down and bottom-up approaches.

The top-down and bottom-up approaches are two main methodologies for flexible electronics manufacturing and they are divided according to the process sequence. The top-down approach generates nano/micro-sized structures by scaling down bulk Si wafers through lithography and etching [135]. In contrast, the bottom-up approach is the reverse of the top-down method, involving the assembly of Si atoms to create nano/microstructures through chemical or physical synthesis (figure 2(d)) [135].

The top-down approach offers remarkable control over dimensions and patterns in nano/micro scale, facilitating the creation of tailored designs by lithography and etching [136]. The primary advantage of this approach is the preservation of the single-crystalline structure of Si, even before and after the conventional lithography and etching processes. The top-down approach allows for preserving the properties of high-quality Si in flexible electronics production [137, 138]. Furthermore, the well-established fabrication process ensures consistent uniformity and a high yield [139–143]. The top-down approaches encompass various transfer methods, including silicon-on-insulator (SOI) [144–149], <111> wafer undercut etching [34, 139, 150–153], metal-assisted chemical etching (MACE) [154–157], epitaxy-free methods [158–161], crack-based exfoliation [162–166], and bonding technology [128, 167, 168].

The bottom-up approach involves precise control over individual atoms or molecules to create intricate structures through self-assembly processes [135]. Unlike the top-down approach, which involves etching larger structures, the bottom-up approach enables precise control at the nanoscale and the production of self-assembly [134, 169]. Additionally, this approach can regulate the thickness of Si easily. Silicon nanomembranes (SiNMs) [170] in 2D systems, silicon nanowires (SiNWs) [171] in 1D systems, and

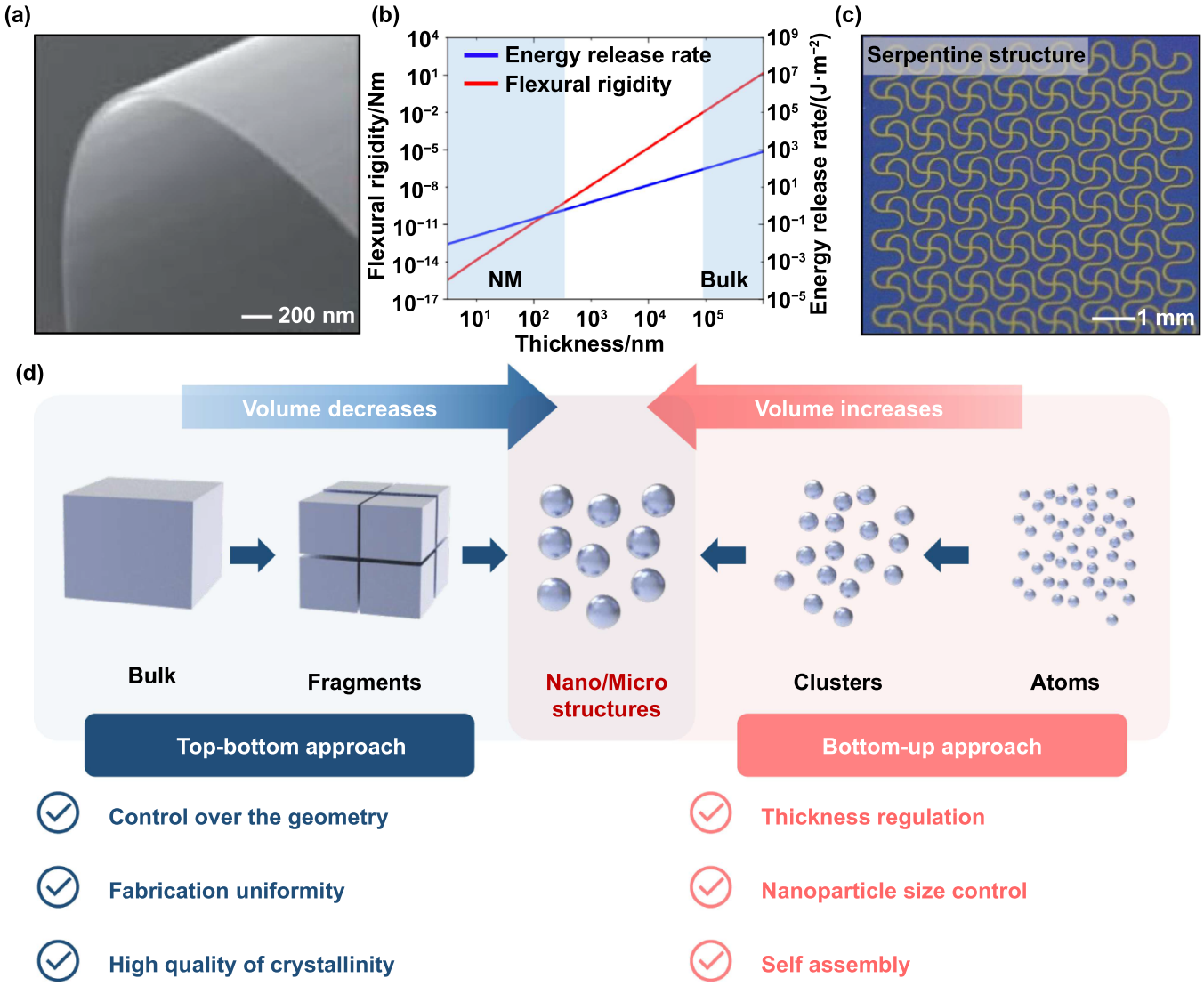


**Figure 2.** Silicon properties and fabrication approaches. (a) High degrees of bendability of nanomembranes image. (b) Flexural rigidity and energy release rate of silicon. Reproduced from [33], with permission from Springer Nature. (c) Serpentine structure for flexible electronics (d) Advantage of top-down and bottom-up fabrication approaches.

silicon nanoparticles [172] in 0D systems can be generated by a bottom-up approach. However, achieving precise manipulation of nanoscale components demands sophisticated techniques and equipment. Additionally, there can be challenges in generating device arrays across large areas [135]. The bottom-up approaches comprise CVD [115, 173–175], physical vapor deposition (PVD) [176], excimer laser annealing [106, 107], aluminum-induced crystallization (AIC) [177–179], and vapor–liquid–solid (VLS) [180–183].

Herein, this review offers the introduction of contemporary trends in Si fabrication methods, spanning a variety of structures and applications. We categorize Si fabrication techniques into top-down and bottom-up approaches, with a focus on their utility in flexible electronics. We explain the development of methods designed for flexible electronics and their applications.

## 2. Top-down approaches

### *2.1. SOI based transfer technique*

SOI is a prominent semiconductor structure comprised of a bottom thick Si substrate layer, a middle silicon dioxide ($SiO_2$) layer, and an ultrathin top Si layer with nano/microscale thickness. One of the top-down approaches utilizing the SOI for flexible electronics is the SOI based transfer technique that utilizes the top single-crystalline Si nano/micro membrane for flexible electronic applications [144–149]. To apply the top Si into flexible electronics, it is essential to separate the top Si layer by sacrificing the middle $SiO_2$ layer. However, the challenge lies in the dissolution of the middle $SiO_2$ layer without damaging the top Si layer while maintaining the superior properties of Si. Typically, materials like hydrofluoric acid (HF) solution or buffered oxide etchant solution exhibit high

reactivity with the middle $SiO_2$ layer, because of producing a combination of water and volatile silicon hexafluoride ($SiF_4$) by-products, which can be easily removed ($SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O$) [184]. However, in the case of Si, the atomic structure characteristics of single-crystalline Si involve the arrangement of Si atoms in a diamond cubic structure, forming a strong and stable network of covalent bonds. This structure results in a lack of reactivity to many chemicals, including HF solution [31]. These etching properties of $SiO_2$ and single-crystalline Si with HF solution permit selective etching of only the middle $SiO_2$ layer, leaving the top Si layer undamaged. Utilizing this selective etching technique, eliminating the risk for material modifications enables the direct use of single-crystalline Si nano/micro membrane in flexible electronics through a transfer process. Furthermore, high-temperature processes such as doping are conducted before the subsequent transfer of the top Si layer, enabling the integration with flexible substrates [185–188]. Also, by employing the conventional lithography processes, the top Si layer can be easily designed, heightening the overall applicability of the Si-based flexible electronics [77, 120, 124, 189, 190].

This approach encompasses three main fabrication processes. **(1) Hole & structure design:** there are two main strategies for transferring the top Si layer onto the flexible substrate. The first strategy involves creating micro-hole patterns in the top Si layer. HF solution can seep through in micro-hole patterns and dissolve the middle $SiO_2$ layer [77, 124, 145]. The second strategy is pre-designing the top Si layer on the SOI wafer before separating the top Si layer from the bottom Si substrate [147, 189, 191]. **(2) Oxide layer undercut:** dissolving the middle sacrificial $SiO_2$ layer process is crucial, during the transfer process [184]. The $SiO_2$ layer, which acts as an adhesion layer between the bottom handling Si substrate and the top Si nano/micro membrane, undercuts using solutions such as HF, allowing the sole transfer of the top Si layer. HF reacts exclusively with the $SiO_2$ layer and negligibly affects the top Si layer, maintaining the properties of the top Si layer [31]. In the first strategy of the micro-hole patterning process, HF solution permeates through the micro-hole patterns and dissolves the $SiO_2$ layer. Each micro-hole serves as an individual entry point for the HF solution. Due to these periodic micro-hole patterns, even when transferring a large area of the top Si layer, the undercut process can be completed in the same duration. Additionally, the entire undercut time is adjusted according to the size of the micro-hole and the interval between each micro-hole, which results in a uniform and efficient etching across a broad sacrificial layer, regardless of its dimension. The second strategy pre-designing the top Si layer facilitates the ultra-thin Si transfer without micro-hole patterns. The $SiO_2$ layer undercut starts from the edges of the designed top Si layer so that while smaller top Si areas require shorter etching times, larger top Si areas necessitate a much longer immersion in the HF solution. **(3) Pick-up with stamp:** after the $SiO_2$ layer is completely etched, the top Si layer detaches from the bottom Si substrate. At this step, a common approach for transferring the top Si layer is the pick-up with the elastomer (e.g. polydimethylsiloxane (PDMS)) stamp. As the elastomer stamp comes into close contact with the top Si layer, van der Waals forces become dominant in the contact layer due to the predominant closeness of the molecules of both surface materials [192–195]. Van der Waals forces are important for the transfer techniques. Covalent and ionic bonds involve the sharing or transfer of electrons, while van der Waals forces are based on temporary electron fluctuations so van der Waals forces have comparatively weaker bonding forces than covalent and ionic bonds [196, 197]. This weaker nature of van der Waals forces makes them suitable for temporarily holding the top Si layer onto the PDMS stamp during the transfer printing process. This temporary bond is crucial for the transfer technique, facilitating the smooth pick-up from a donor substrate and subsequent release of the top Si layer onto a target flexible substrate. The adhesive materials used on flexible substrates include polyimide (PI), SU-8, and Norland optical adhesive, etc. These materials bond with Si, easily breaking the van der Waals forces between PDMS and the top Si surface and ensuring the efficient transfer printing process (figure 3(a)). In this section, the SOI based transfer technique utilized $SiO_2$ layer as a sacrificial layer for transfer printing the top Si layer of SOI. However, considering future approaches for thin-film nanoelectronics transfer printing, it is essential to develop methods for transferring without chemical for dissolving a sacrificial layer. This advancement would pave the way for low-cost, green approaches for future transfer printing technique [198–201].

The SOI based transfer techniques have the novel advantage of using single-crystalline SiNMs. SiNMs are transferred onto flexible PI substrates through the hole transfer method, leading to the fabrication of Si-based flexible strain sensors [124]. These Si-based flexible strain sensors have a high gauge factor (GF) due to the piezoresistive effect, compared to conventional metal-based strain sensors [203, 204]. The piezoresistive effect is the resistance change of the semiconducting materials depending on the applied strain. When strain is applied, semiconducting materials bandgap changes, leading to a redistribution of carriers. This affects the mobility and effective mass of carriers. The resistance alteration due to the piezoresistive effect is several times larger than that resulting from the geometrical changes. Consequently, the Si-based strain gauge has superior GF (around 100) compared to the metal-based strain gauge. Furthermore, in this research, the strain gauge was designed in a serpentine structure to enhance the response of strain in a specific direction. Two strain gauges were positioned in each vertical and horizontal directions. By using a certain doping concentration, the strain gauges minimally respond to temperature while maintaining the response of strain. The substrate was also etched in a serpentine structure to make the device stretchable, thereby the device can consistently measure small face muscle movements over extended periods, even if the facial skin moves or stretches a lot.

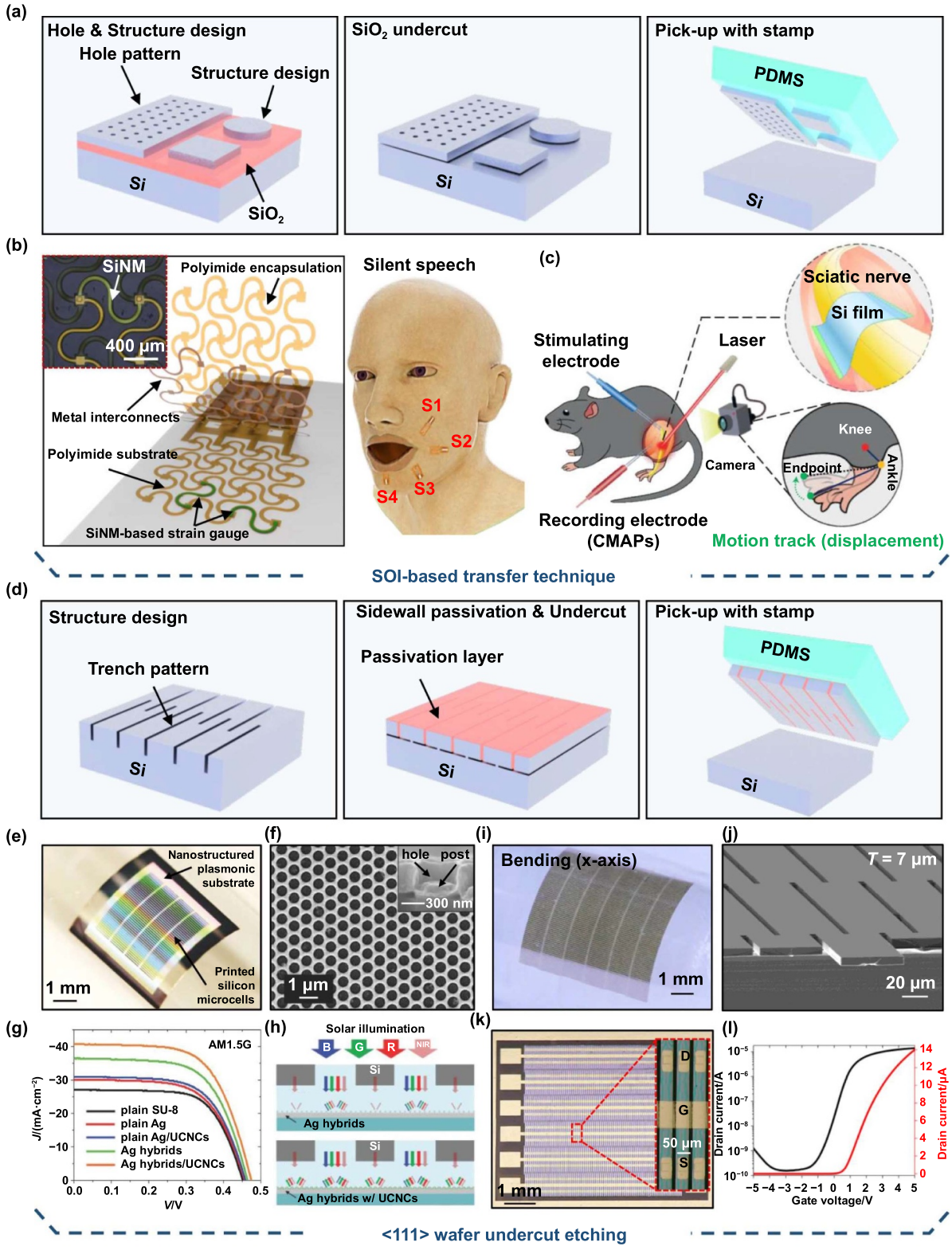


**Figure 3.** Silicon-on-insulator (SOI) transfer method & <111> wafer undercut etching. (a) Fabrication process of SOI transfer method. (b) Silicon based strain sensors for silent speech recognition system. Reproduced from [124]. CC BY 4.0. (c) Thin-film silicon diodes for the optoelectronic of neural activities. Reproduced from [189], with permission from Springer Nature. (d) Fabrication process of <111> wafer undercut etching. (e) Ultrathin nanostructured silicon solar microcells. (f) SEM image of nanostructured plasmonic substrate. Inset shows hole/post of nanostructure. (g) Representative *J*–*V* curves of silicon solar microcells at various substrate configurations. (h) Illustration of optical processes of solar illumination. [202] John Wiley & Sons. © 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (i) Photograph image of ultrathin nano and micro membranes of crystalline silicon sheet. (j) SEM image of interconnected silicon microcells with a thickness of 7 $\mu$m. (k) An optical image of transistors fabricated by SiNM sheet. (l) Transfer characteristics (ID-VGS) of transistor. [46] John Wiley & Sons. © 2023 Wiley-VCH GmbH.

These Si-based strain gauges affixed near the muscles surrounding the mouth, detect the minute muscular changes associated with different word pronunciations, thus enabling silent speech recognition with deep learning based data processing (figure 3(b)).

Next, as a notable biomedical application, a bioresorbable thin-film Si diode was developed [189]. This device fabrication process is different from the previous micro-hole transfer technique. Instead of designing the top Si layer after transferring it to a flexible substrate, the Si was etched in a pre-designing structure on the SOI wafer without micro-hole patterns. Also, before the pre-designing process, the top Si layer is turned into different junctions by different doping processes. The fabricated $p^+n$ or $n^+p$ junction diodes react with lasers differently, enabling either *in vivo* excitation or inhibition of peripheral and central nervous systems. The optoelectronic device is completely fabricated on the SOI wafer, therefore there is no need for any extra fabrication processes after being transferred to a flexible substrate. Furthermore, the unique property of Si is biodegradable and biocompatible in the human body, eliminating the need for additional surgeries to extract the device after insertion. ($Si + 4H_2O \rightarrow Si(OH)_4 + 2H_2$) [205–208]. These Si-based bioresorbable diodes enable the optoelectronic excitation and inhibition of peripheral neural activities for hindlimb movements (figure 3(c)).

### 2.2. *<111> wafer undercut etching*

The biggest downside of the thin film transfer techniques based on SOI is that the price of SOI wafers is much higher than that of single-crystalline Si wafers [34, 46]. Recently, a Si <111> wafer anisotropic undercut etching technique has been employed to transfer an ultra-thin Si layer from the mother wafer, aiming to achieve cost efficiency [34, 46, 139, 150–153]. This technique leverages the inherent orientation characteristics of the <111> Si wafer. Si is etched at a faster etching rate in the <110> direction compared to the <111> direction. Since the <111> direction of Si has more backbond surface states and fewer dangling bonds, the etching rate of the <111> direction is much slower than the <110> direction [209, 210]. The increased backbond surface states make it more mechanically stable and the lower density of dangling bonds reduces the number of reaction atoms, resulting in less reactive sites for the etching solution like tetramethylammonium hydroxide (TMAH) or potassium hydroxide (KOH) solutions [209–211]. Utilizing this selective etching property makes it possible to transfer the single-crystalline Si membrane in pristine condition similar to the SOI transfer technique. The advantage of this method is the separation of high-temperature processes in the post-transfer process. Furthermore, while the SOI has the initial thickness of the top Si layer, this method offers the advantage of adjusting the thickness of the Si membrane based on the depth of the trench pattern. Especially, the SOI based transfer technique has a single-use limitation because of a single $SiO_2$ sacrificial layer. However, this Si <111> wafer-based transfer technique uses the Si as a sacrificial component, allowing for multiple transfers of ultra-thin Si layers from the mother Si wafer. After completing a single transfer process of Si membrane, the mother wafer can be planarized using TMAH or KOH solutions that etch Si in an anisotropic direction, enabling the wafer reuse for the next transfer cycle by polishing the mother wafer surface. These multiple generations of Si membranes can be repeated until the mother wafer is fully consumed, enhancing the cost efficiency significantly [34, 46, 153].

This Si <111> wafer undercut etching consists of three main fabrication processes. **(1) Structure design:** by using the aforementioned characteristics of the Si selective etching property, the Si membrane needs to be undercutted to <110> plane direction. Therefore, a trench line has to be patterned perpendicularly to the <110> direction on the Si <111> wafer. This ensures that the <110> plane is exposed to the Si etching solution, leading to an anisotropic wet chemical etching undercut [34, 150]. The trench design allows for adjusting the width and thickness of the transferred Si membrane by controlling the distance between the trench lines and the etching depth of the trench lines. For designing the trench lines, Si is etched using a deep reactive-ion etching (DRIE, Bosch Process) system for anisotropic etching, resulting in a high aspect ratio between the trench and sidewall [212, 213]. **(2) Sidewall passivation & undercut:** for undercutting the Si membrane, the bottom area of the trench lines is exposed to TMAH or KOH solutions. At the same time, the trench sidewall needs to be passivated with materials, such as thermally grown $SiO_2$ (t-$SiO_2$) and silicon nitride ($Si_3N_4$) that are chemically stable from these Si etching solutions [214, 215]. These passivation materials have dense and stable network structures, which can effectively prevent the penetration of etchants due to their high resistance to chemicals. The undercut is conducted through a selective etching process, wherein the etching rate in the <110> direction is faster than that in the <111> direction. Nonetheless, the etching in the <111> direction cannot be negligible. When the overall process time of undercut is increased due to the wider interval between the trench lines, the thickness reduction to <111> direction increases, resulting in the challenge of maintaining the desired thickness of the Si membrane [34]. In conclusion, to produce ultra-thin SiNMs, it is essential to manage the interval between the trench lines and the etching depth of the trench lines accurately. **(3) Pick-up with Stamp:** following the complete bottom undercut, the top Si membranes are detached using an elastomer (e.g. PDMS) stamp. Same as the SOI transfer technique, the top Si layer leads to conformal contact on an elastomer stamp, by the van der Waals adhesion force occurring at the interface [192–195]. The detached Si membranes are transferred onto a flexible substrate using an adhesion layer similar to the previous SOI method (figure 3(d)).

Employing this technique, Si microcell-based solar cells were fabricated (figure 3(e)) [202]. The advantage of the Si solar microcell fabrication based on the <111> wafer undercut etching is that after performing the bottom undercut process, the remaining passivation layer for undercut allows for an additional bottom doping process [151, 153, 202]. In the

Si solar microcell created by the bifacial doping process, both surfaces serve as pathways for photogenerated carrier collection, leading to enhanced power conversion efficiency [216–218]. This approach not only reduces the series resistance, which is critical for the charge movement but also ensures that both the front and back surfaces actively contribute to the electron and hole carriers collection process. This dual-surface results in more efficient carrier collection across the entire microcell, significantly improving the overall performance. However, in the case of SOI based transfer technique, only the top surface of the Si can be doped in one type (n-type or p-type) because of the presence of the $SiO_2$ layer. Therefore, the Si <111> wafer undercut etching process that enables doping both the top and bottom surfaces in different types can be further used for the fabrication of more diverse electronic devices. Also, since the top Si layer thickness of the SOI wafer is a product specification, it is impossible to achieve the desired Si layer thickness. However, in the case of this technique, the Si microcell thickness can be varied widely on the microscale by adjusting the etching depth of the trench line. This article utilized these advantages of <111> wafer undercut etching technique to produce high-performance flexible nanostructured Si solar modules. Additionally, the fabricated printable form of the ultrathin single-crystalline Si microcells can be easily transferred to various bottom substrates, enabling the improvement of solar cell performance. Specifically, through a soft lithographic molding process, they employed a nanostructured plasmonic substrate as the bottom substrate (figure 3(f)), achieving a 130% performance increase compared to a bare Si solar microcell (figures 3(g) and (j)).

Traditionally, this approach was used to fabricate micro and nano Si ribbons or microcells [151, 153, 202]. Recent advancements have expanded this technique to develop transferred Si membranes in sheet forms [46]. Si microcells were connected through interlocking and anchoring connections to create a sheet structure of Si nano/micro membrane (figures 3(i) and (j)). By partially doping the source-drain region before the undercut etching process, there's no need for a high-temperature process after the transfer on the flexible substrate. Using this method, 471 individually operating n-type metal-oxide-semiconductor field-effect transistor (MOSFET) arrays were fabricated within a 5 mm × 5 mm SiNMs sheet (figure 3(k)). The performance of each transistor showed a $V_{th}$ of 0.038 V, an on/off ratio greater than $10^6$, and mobility of 241 $cm^2 \cdot V^{-1} \cdot S^{-1}$ (figure 3(l)). The sheet form of these interconnected microcells shows promising further potential applications for low-cost flexible devices in the future.

### 2.3. Metal-assisted chemical etching (MACE)

The MACE process involves using a patterned metal layer (e.g. gold (Au), platinum (Pt), and silver (Ag)) as a catalyst for a local redox reaction to etch a metal-coated Si in a solution such as HF. Si exhibits little reactivity with HF due to its crystalline structure. However, by applying a metal layer to Si, the catalytic response of the metal can be utilized to facilitate Si etching at the Si/metal interface. This approach enables anisotropic etching, thereby allowing for a high aspect ratio. Moreover, since the process is conducted at room temperature, the risk of metal contamination is minimal [219]. The MACE is a process of wet etching Si using a metal catalyst and is used to form SiNWs and porous Si structures [154, 220, 221]. Specifically, using the metal catalyst layer with the porous pattern, SiNWs can be created by using the MACE process. The periodic arrangement of SiNWs with radial junctions enhances light absorption while preserving the advantages of reduced reflection and effective light trapping. Due to the low reflection and strong absorption properties of SiNWs, it is extensively employed as an active layer in solar cells [222]. Additionally, in the case of SiNWs fabrication, unlike the typical bottom-up approach, SiNWs fabricated by the MACE method can be produced without the need for infrastructure for crystal growth, making it cost-effective by canceling material costs associated with the etching process. On the other hand, the nanoporous Si structure can be created using a solution composed of $AgNO_3$ and HF, eliminating the need for metal layer deposition [156, 223]. The porosity of the nanoporous Si is influenced by various factors such as the doping concentration of Si, temperature, etching time, and the composition of the etching solution [224]. When this nanoporous structure is applied to Si needles for intratissue injection, it offers enhanced safety and controlled biodegradability. Consequently, these porous Si nanoneedles can effectively load nanoparticles and accurately target their release to specific, shallow areas of the tissue [225, 226]. The MACE process can form precise structures with high aspect ratios and high cost efficiency [156].

This process involves depositing polystyrene (PS) beads and metal layer, lift-off, and etching. **(1) Deposit PS beads & metal layer:** to create a metal mask for Si etching, nanostructures such as PS beads are used [227]. A colloid solution containing PS beads is spin-coated and plasma processes are employed to control the size of these nanostructures. In this process, PS beads are formed through a self-assembly process, creating a densely packed hexagonal shape of nanospheres [228]. Since the spacing between these spheres is very tight, the size of PS beads needs to be reduced for wire formation through a plasma etching process. Subsequently, a thin metal layer is deposited by an electron-beam (e-beam) evaporator [154]. **(2) Lift-off PS beads:** a lift-off process is employed to dissolve the PS beads with PS etchant such as chloroform, thereby exposing the areas of Si not covered by the metal layer. This method facilitates the creation of nanoporous metal patterning [154]. **(3) Etch Si:** MACE is a process that utilizes metal as a catalyst to promote Si etching. The solution used for MACE primarily consists of HF and $H_2O_2$. After the metal layer surface is exposed to the solution, the reduction occurs caused by $H_2O_2$ at the metal surface. The hole generated by the reduction reaction of $H_2O_2$ reaches the Si/metal interface and oxidizes the Si, forming silica ($SiF_4$). Subsequently, this silica is dissolved by HF. Through repeated redox reactions, the Si at the Si/metal interface is anisotropically etched (figure 4(a)) [223].

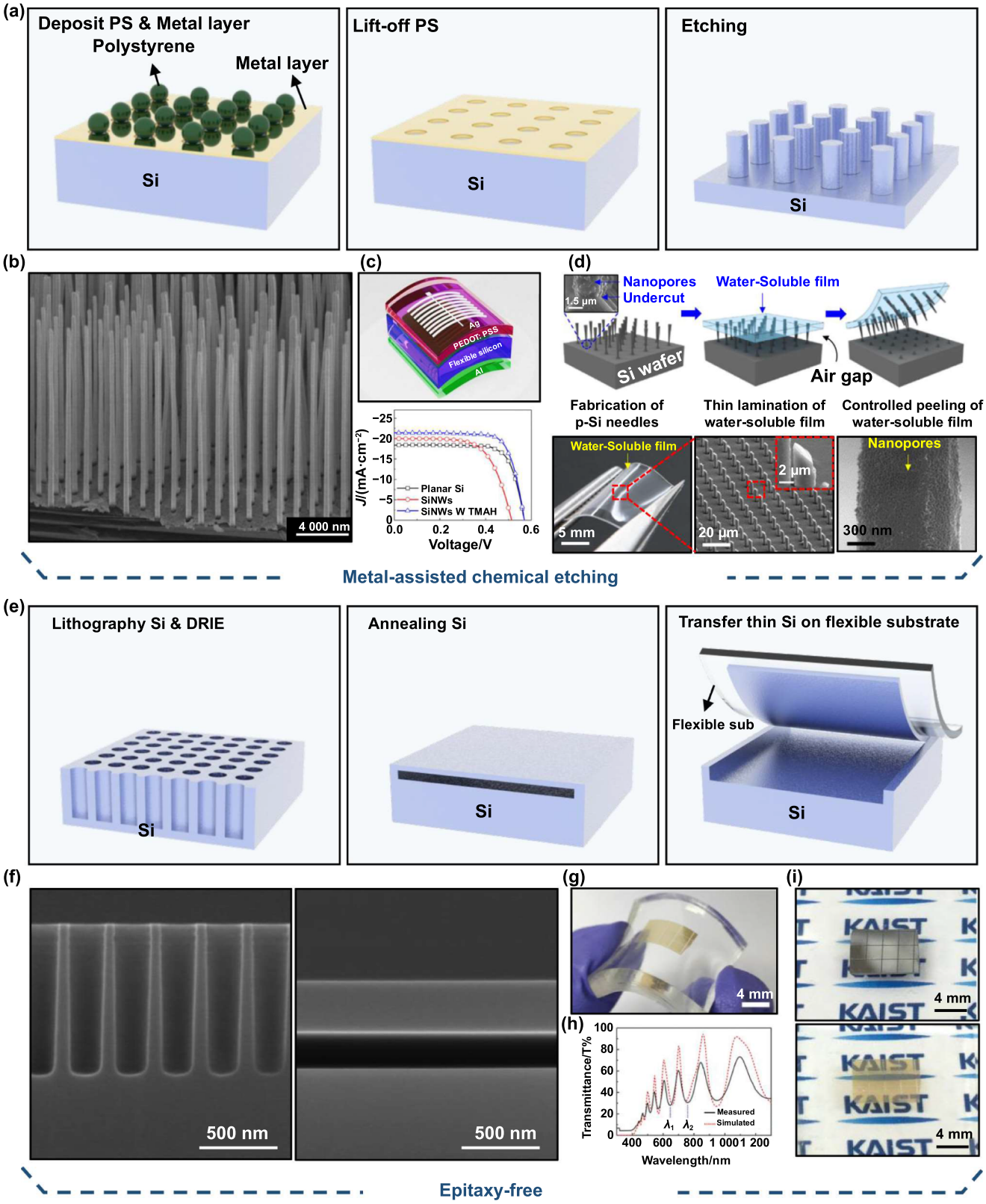


**Figure 4.** Metal assisted chemical etching (MACE) and epitaxy free. (a) Fabrication process of MACE method. (b) SEM image of SiNWs fabricated by using MACE process. [229] John Wiley & Sons. © 2020 Wiley-VCH GmbH. (c) Schematic structure and current–voltage curve of the flexible hybrid solar cell. Reprinted with permission from [230]. Copyright (2017) American Chemical Society. (d) Schematic structure of the p-Si needles and SEM image of nanopores formed on the surface of p-Si needles. Reprinted with permission from [231]. Copyright (2020) American Chemical Society. (e) Fabrication process of epitaxy-free. (f) SEM images of Si pores and the layer based on silicon on nothing structure. (g) Flexibility of ultrathin Si film transferred by using epitaxy free. (h) Graph of transmittance measurements of Si film using the Petterson and Peumans models. (i) Optic images of the mother wafer and Si film which is transferred on PDMS. Reprinted with permission from [232]. Copyright (2016) American Chemical Society.

(Cathode (metal layer): $H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$, $2H^+ + 2e^- \rightarrow H_2\uparrow$; Anode (Si): $Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+$, $SiF_4 + 2HF \rightarrow H_2SiF_6$; Overall equation: $Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_2\uparrow$).

By adjusting the reaction time during the etching process, it is easy to control the aspect ratio of the nanostructure. Upon completion of the etching process, the metal mask is removed using a metal etchant, resulting in the production of Si nanostructures (figure 4(b)) [229, 233]. To apply the fabricated Si nanostructure to flexible electronics, a thin Si wafer was employed to utilize the thin Si nanostructure directly. In a different approach, PDMS was spin-coated onto the fabricated nanostructure for mechanical support and electrical insulation. Subsequently, the Si substrate was detached from the nanostructure [230].

A high-performance flexible Si-based solar cell was fabricated using SiNWs through MACE process [233]. In this research, the 14 $\mu$m Si film was obtained by reducing the thickness of the Si wafer using KOH, thereby making the Si film flexible [234]. However, reducing the thickness led to a decreased light absorption capacity of Si, passing through more than 10% of visible light. To compensate for the light absorption capacity, the structures of SiNWs are applied to the flexible Si film. The SiNWs have a relatively low reflectance across a wide range of solar spectrum wavelengths, resulting in more efficient light absorption compared to the same volume of planar Si. However, these nanostructures significantly increase the surface area of the Si, potentially inducing surface trap states, which can lead to higher recombination rates at the surface and significant degradation in the performance of photovoltaics [233]. To prevent this degradation and ensure a long lifespan, surface passivation strategies are necessary [235–237]. In this research, to reduce carrier recombination caused by the increased surface area of SiNWs structure, anisotropic etching with TMAH was employed [238, 239]. After TMAH treatment, only the bottom portion of the SiNWs structure remained, leading to a decrease in the density and aspect ratio of nanostructures, resulting in a small reduction in overall light-trapping characteristics [240]. While the untreated SiNWs structure exhibited lower performance due to recombination, the TMAH-treated SiNWs structure demonstrated higher performance, along with improved light absorption compared to planar Si (figure 4(c)).

Nanoporous structures fabricated by the MACE process were employed for controlling drug delivery and degradation of the Si nanoneedles [231]. In this research, the Si nanoneedles were fabricated by photolithographic patterning and DRIE process on the bulk Si wafer. Subsequently, utilizing the MACE process, nanoporous structures were formed on the Si nanoneedles. The porosity of Si nanoneedles was controlled by the etching time of the MACE, which allowed for adjusting the drug loading capacity and programmable dissolution rate (figure 4(d)). When rigid bulk Si wafers, on which Si nanoneedles were fabricated, are used as a back substrate, a mechanical mismatch occurs at the soft tissue and rigid device interface [241]. To address this issue, this study successfully resolved the rigidity problem by peeling off the Si nanoneedles with the flexible substrate, water-soluble film. The completed porous Si nanoneedles were implanted within the tissue without hindering the wearer's natural movement due to the flexiblesubstrate and ensured prolonged drug release through the covalent bonding of drug cargo on the porous structure surface with gradual biodegradation.

### 2.4. Epitaxy-free

Another method for depositing thin Si film, used in the fabrication of flexible solar cells, is commonly achieved through an epitaxial deposition process [242, 243]. However, this epitaxial deposition process requires significant Si consumption, requiring high production costs. To resolve this issue, the epitaxy-free process has been developed for transferring thin Si at a lower cost without the epitaxy process. Epitaxy-free is related to the principle of creating voids through empty space in silicon (ESS) based on the microstructure transformation of silicon (MSTS) technique. The MSTS technique involves annealing the Si substrate in a non-oxidizing environment such as hydrogen ambient. This annealing process triggers a self-organizing migration of the Si surface in a way that minimizes surface energy [244, 245]. Notably, when Si has a deep trench pattern of circular shape, the empty space of a spherical void starts from the bottom surface of the trench, where the radius of curvature is the lowest [246]. Through this technique, the shape of the ESS is adjusted based on the arrangement of trenches [158]. For example, when forming a single trench, it transforms into a spherical empty space, and when creating a row of trenches, a pipe-shaped empty space can be formed. In particular, when trenches are manufactured in a lattice structure, a plate-shaped empty space is formed. Consequently, the silicon-on-nothing (SON) structure is fabricated, featuring a thin Si film located above the plated-shaped void. The SON structure offers the advantage of controlling thickness based on the trench depth and is more cost-effective than SOI due to lower material consumption and a simple fabrication process [159].

This process can be explained in three key steps. **(1) Lithography & DRIE:** the configuration of the trench array significantly impacts the uniformity of the thin Si film in the SON structure. An aligned trench array ensures uniform thickness of the thin Si film, while randomly arranged hole patterns lead to the formation of defects during the annealing process, which disrupts the uniform formation of the thin Si film. Therefore, the trenches have the same aspect ratio and spacing. The trench array is created on a Si substrate through a lithography process, followed by an anisotropic etching of Si using DRIE [247, 248]. The size and depth of the trench are important parameters for adjusting the thickness of the thin Si film in the SON structure [249]. When the trench depth becomes too deep, voids can form in multiple layers. Therefore, an aspect ratio of 9.5 or lower is necessary to prevent multilayer formation [250]. Additionally, increasing the trench size leads to an increased thickness of the Si film. However, since the annealing time is proportional to the fourth power of the diameter, a large trench diameter results in significantly extended

process times. As a result, adjusting these parameters is essential appropriately to achieve the desired film thickness [159]. **(2) Annealing:** to fabricate the thin Si film, the trench array is merged or combined through the sufficient mobility of Si atoms [249]. To provide sufficient mobility of Si atoms, a non-oxidizing environment (e.g. $H_2$ or Ar ambient) and high temperature over 1100 °C are required in the annealing process. Non-oxidizing environment can reduce the oxidizing impurities, ensuring the dangling bonds at the trench surface. High temperatures over 1100 °C can increase the mobility of Si atoms, enabling the trench transformation [249]. Additionally, precise pressure control of the interior void is necessary to prevent film deformation. When the pressure in the interior void is different from the atmospheric pressure, the thin Si film is bent or resealed after completing the annealing process. Consequently, the reconfiguration of the trench array leads to the production of SON [159]. **(3) Transfer Si layer:** to utilize the thin Si film in the SON structure for flexible electronics, the thin Si film is separated from the SON wafer using a PDMS substrate. The transfer of the entire Si film is applied to the PDMS substrate by oxygen plasma treatment to enhance the bonding force between the Si and PDMS surface. During this process, the presence of a void in the SON structure allows for facilitating easy separation (figure 4(e)) [251].

An epitaxy-free process was used to create an ultrathin single-crystalline Si film that is both semitransparent and flexible [232]. Traditional photolithography processes struggle to control trench diameters and pitches at the nano-scale. This limitation prevents the reduction of Si film thickness to below the micrometer scale, which is necessary for transparent applications such as displays, wearable devices, and photovoltaics [252–256]. In this research, the trench size was significantly reduced to a 200 nm diameter and a 300 nm pitch using thermal nanoimprint lithography (NIL). This allowed for the thin Si membrane, created through an annealing process, to be reduced in thickness to between 330 nm and 470 nm (figure 4(f)). Additionally, a porous Si was formed in a 2 mm × 2 mm area. This step was crucial to prevent the floating thin Si membrane from collapsing during and after transformation. To achieve sufficient flexibility and semitransparency, a transparent and flexible PDMS film was used to transfer the thin Si film onto the PDMS substrate (figures 4(g)–(i)). The transferred Si film demonstrated excellent mechanical flexibility when reduced to a thickness of less than a few micrometers. It also showed improved transparency on the PDMS substrate, highlighting its potential for broad applications in displays and sensors.

### 2.5. Crack-based exfoliation

In the field of flexible electronics, a crack-based exfoliation method has been developed for applying a large area of single-crystalline Si onto a flexible substrate, eliminating the need for any photolithography or etching processes [162]. The feasibility of crack-based exfoliation technique is significantly influenced by the fracture toughness of the target semiconductor substrate. Fracture toughness, which refers to the ability of a material to resist fracture, governs the criteria for crack growth. This process involves the physical breaking of adjacent atomic bonding in such brittle materials through the formation of cracks. One of the fracture modes occurs when a tensile strained film is attached to the surface of the semiconductor substrate, with the crack propagating parallel to the boundary between the surface and the substrate. This crack is determined by both pure opening stress (Mode 1) and shear stress (Mode 2), and it follows a path during its propagation where the shear component is minimized (figure 5(a), inset). When the stressor layer induces compressive stress, the crack propagates upward, leading to damage to the film, and when it induces tensile stress, the crack tips point toward the interior of the substrate. Due to this flow, the equilibrium depth of the crack needs to be located at a position where mode 2 stress is zero beneath the interface between the film and the substrate [257, 258]. To expand the application areas of this exfoliation technique, research has been conducted on utilizing a metal stressor layer to induce spalling, making it feasible to perform the process at room temperature [162]. This method provides the advantage of controlling the depth of fracture by regulating the thickness and stress of the stressor layer, allowing for easy control of film thickness within the range of 10 $\mu$m to 80 $\mu$m. As the thickness of the stressor layer increases, the stress transferring from this layer to the Si decreases. The stress distribution caused by lattice mismatch between the semiconductor substrate and stressor layer surface increases, leading to an increase in the thickness of the spalled layer [166, 259]. In this process, a handling layer such as PI tape is typically used to adhere to the stressor layer and separate spalling Si from the Si substrate [162]. This process is cost-effective due to the low cost of the plating solution used in depositing the metal stressor layer and the reusability of materials [260].

This process involves depositing a bonding layer, transferring the flexible substrate to the bonding layer, and then applying controlled mechanical stress to exfoliate the thin Si film from the original substrate. **(1) Deposit stressor layer:** the metal stressor layer plays a crucial role in determining crack transfer and depth of spalling Si. Nickel (Ni) is well-suited for metal stressor layers due to its high fracture toughness and the ease with which stress can be controlled through sputtering or electroplating deposition [263]. In the sputtering process, the stress of the Ni thin film can be adjusted by varying the argon (Ar) gas pressure during deposition. Specifically, deposition at low Ar pressure induces compressive stress in the Ni film due to the atomic peening effect, while high Ar pressure induces tensile stress. Also, Ni film can be deposited through electroplating, a method known for its cost efficiency and high throughput compared to sputtering [264]. The residual stress of the Ni stressor layer deposited using electroplating is influenced by both the deposition current density and the chemical composition of the electrolyte. Intrinsic stress in the Ni film exhibits compressive stress at low deposition current density and tensile stress at high current density. The chemical composition also affects the Ni film, with an increase in phosphorous ions in the electrolyte solution correlating with higher tensile stress in the Ni film. Therefore, the stress of the Ni film can be easily adjusted through the sputtering and electroplating processes, making it suitable for the

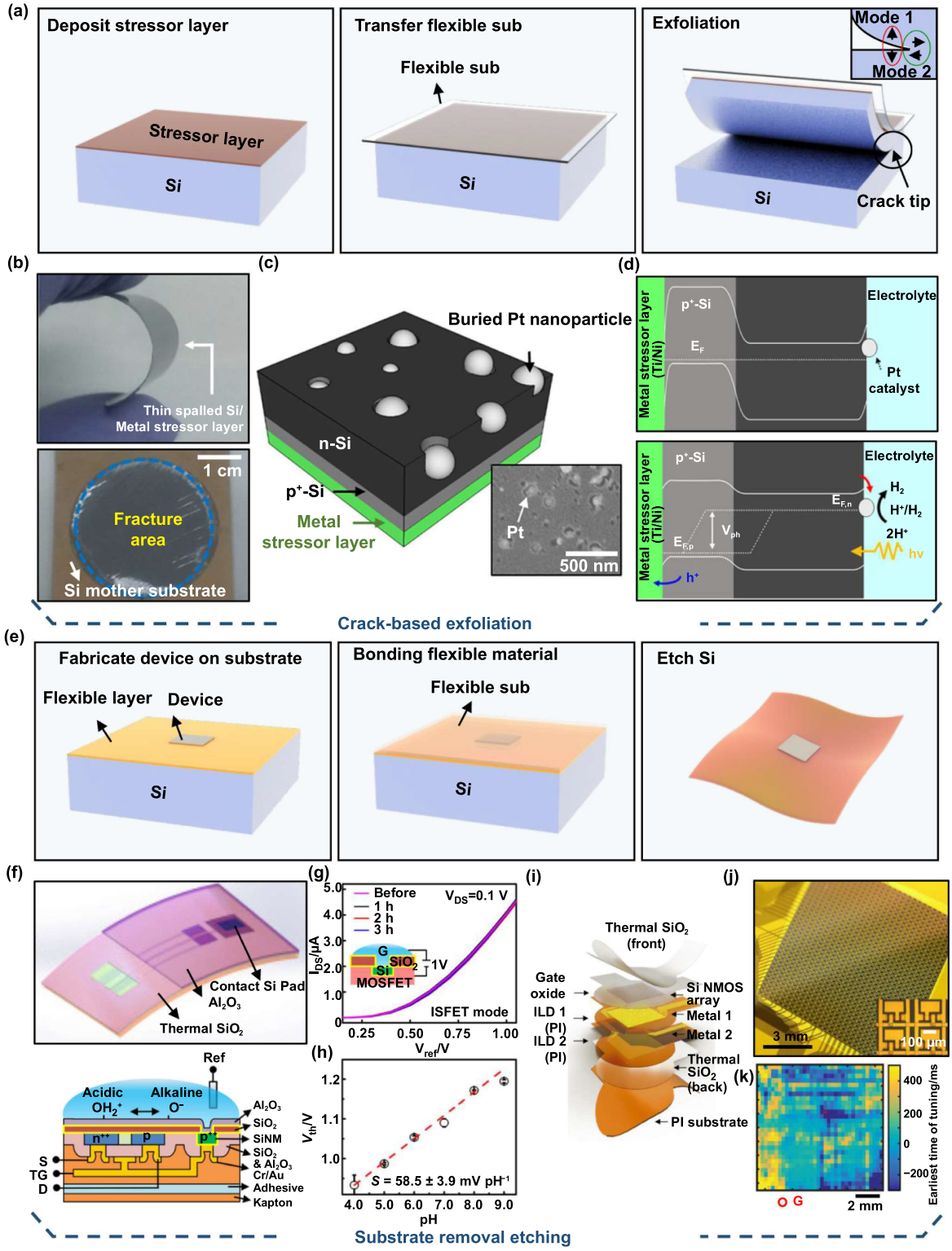


**Figure 5.** Crack based exfoliation and substrate removal etching. (a) Fabrication process of crack-based exfoliation. (b) Flexibility of thin spalled Si/Metal stressor layer and Si mother substrate. (c) Schematic structure of spalled Si layer with Pt nanoparticles and SEM image of Pt nanoparticles. (d) Energy band image of the spalled Si in the dark and illumination. Reprinted with permission from [260]. Copyright (2018) American Chemical Society. (e) Fabrication process of substrate removal etching. (f) Schematic structure of waterproof FET sensors for pH sensing. (g) Measurements of transfer characteristics for a device in ion-sensitive FET (ISFET) mode, captured at intervals during the application of a static bias through a liquid gate (VGS = 1 V) at 1, 2, 3 h. (h) pH sensitivity of the device in response to buffer solutions from 4.0 to 9.0 pH. Reprinted from [261], © 2022 Elsevier B.V. All rights reserved. (i) Schematic picture of a flexible neural sensing system utilizing thermal $SiO_2$ as the encapsulation layer. (j) Photograph of a neural matrix array with 1008 channels. (k) A spatial map of the time window when directional tuning became statistically significant for each electrode, revealing the temporal evolution of directional information. The red circle denotes the position of the sample electrodes from letter G. From [262]. Reprinted with permission from AAAS.

metal stressor layer. By adjusting both the stress and thickness of the Ni layer, the thickness of spalling Si can be easily controlled [166, 259]. **(2) Transfer flexible substrate:** the handling layer is employed to prevent damage to the brittle Si film after the transfer process. There are two methods for utilizing the handling layer: using the Ni layer itself, which serves as a metal stressor layer, or employing a flexible substrate by bonding on the stressor layer. The Ni layer serves as a handling layer to assist the separation of thin Si by applying external force. Additionally, a flexible film, such as PI tape, is also used as a flexible substrate by bonding the film onto the metal stressor layer [265]. **(3) Exfoliate Si:** after the handle layer is applied, a crack is created at one edge of the wafer to allow the spalling process to proceed. There are various methods to exfoliate Si films. The first method involves applying heat to the stressor layer and substrate through the annealing process, inducing thermal misfit stress. The difference in thermal expansion coefficients between the stressor layer and the substrate leads to thermal mismatch stress, resulting in crack formation. Another approach involves pretreating the Si substrate with a laser before depositing a metal stressor layer. This laser process forms a crack without damaging the Si surface, and this initial crack expands and propagates in a direction parallel to the Si surface. Additionally, the controlled spalling process can be employed to utilize external force for initiating crack. When an external force is applied in the direction of pulling one edge of the handling layer above the metal stressor layer upward, a crack initiates at the edge of the Ni stressor layer, causing the upper Si layer to completely peel off. Consequently, the thin Si layer is transferred on the flexible substrate (figure 5(a)) [162, 266].

The crack-based exfoliation technique was employed to produce a cost-effective and high-performance photoelectrochemical (PEC) cell. Water splitting in PEC processes has gained attention as a technology for converting solar energy into a clean energy carrier, hydrogen [267, 268]. An efficient approach for the conversion of solar energy into hydrogen is to use semiconductors with an appropriate bandgap that efficiently absorbs visible light and band edge positions suitable for water-splitting reactions. Traditionally, materials like Si and gallium arsenide (GaAs) have been used as photoelectrodes in PEC, as they have bandgaps low enough to facilitate efficient hydrogen evolution reactions (HERs) [269–272]. However, the use of conventional Si and GaAs substrates has been limited due to the high manufacturing costs [271, 273]. To address these limitations, research has focused on methods to produce thin Si and GaAs layers, reducing the use of expansive materials [271]. For producing a thin Si layer, the traditional diamond wire sawing method allowed for the production of 60 $\mu$m thick Si but led to significant material loss [274, 275]. To overcome these challenges, a crack-based exfoliation process was developed, resulting in the production of thin Si layers with thickness ranging from less than 5–50 $\mu$m, significantly reducing manufacturing costs (figure 5(b)) [276]. In this research, utilizing the crack-based exfoliation technique, the thin $np^+$ junction Si is fabricated for PEC application. The $np^+$ junction was formed on the n-type Si surface through a boron ion implant doping process. To prepare the stressor layer for spalling Si, a seed layer composed of Ti/Ni was deposited on the Si surface using an e-beam evaporator [260]. The Ti layer serves as an adhesion layer for the Ni stressor layer and the Ni stressor layer was electroplated on the Ni seed layer. An external force was applied to initiate the generation of crack and to propagate the crack parallel to the surface of the mother Si substrate (figure 5(c)). To construct a high-performance PEC cell, a highly efficient catalyst is required. Si itself has low catalytic activity for the HER. To address this issue, Pt nanoparticles were used as a catalyst. The band diagrams of 16 $\mu$m thick spalled $np^+$ Si with Pt nanoparticles were measured under both dark and illuminated conditions. Under illumination, splitting occurs between the electron ($E_{f,n}$) and hole quasi-Fermi level ($E_{f,p}$). This difference represents $V_{ph}$, and the generation of $V_{ph}$ induces band bending facilitating the electron transfer to the Si/electrolyte interface easier, occurring the HER (figure 5(d)). Consequently, a thin Si $np^+$ junction that can be used as a PEC HER was obtained cost-efficiently through a crack-based exfoliation process.

### 2.6. Substrate removal etching

In the case of the SOI based transfer technique, to use the top Si layer for the flexible electronics, the fabrication process involves etching the sacrificial $SiO_2$ layer to transfer the top Si layer to the flexible substrate using an elastomer stamp. However, this method has the disadvantage that unwanted micro-holes are created in the top Si layer, or the high-quality t-$SiO_2$ encapsulation layer cannot be used in flexible electronics due to the HF solution. To address these limitations, a substrate removal etching method based on the SOI wafer has been developed. This method involves manufacturing a device using single-crystalline Si on a rigid SOI handling wafer, bonding a flexible substrate to the surface of the completed device, and then removing the rigid handling bottom Si substrate. Therefore, the single-crystalline Si can be used without micro-holes in flexible electronics and the t-$SiO_2$ layer can be utilized in device encapsulation due to the absence of using HF solutions. Additionally, since the device is fabricated on a rigid SOI wafer, high-temperature processes can be performed, such as doping, oxidation, and deposition. Specifically, the use of the t-$SiO_2$ layer as an encapsulation layer for implantable bio-electronics increases the device lifespan to several decades [128]. Through an accelerated test using phosphate-buffered saline (PBS), it was found in the research that the t-$SiO_2$ thickness of 100 nm maintained encapsulation for nearly 20 days at a temperature of 70 °C, with a reduction of 5 nm per day. Transformed by the Arrhenius equation, at pH 7.4, and 37 °C the dissolution rate of $SiO_2$ is $4 \times 10^{-2}$ nm·d$^{-1}$, indicating an exceptionally long lifespan of around 70 years [128]. Also, t-$SiO_2$ with a very low water transmission rate of $1.53 \times 10^{-3}$ g·m$^{-2}$·d$^{-1}$ at 85 °C and 500 nm thickness which significantly increases the lifespan even in harsh environments, can serve as an excellent encapsulation layer [277]. Consequently, the substrate removal etching process enables to use of single-crystalline Si without deformation and t-$SiO_2$ as an encapsulation layer, which not only extends the lifespan

of the flexible electronics but also allows to maintain performance even in harsh environments.

This process encompasses the deposition of a device on the Si/PI substrate, transferring a flexible substrate to the substrate, and etching the Si substrate to release the device. **(1) Fabricate device on Si/flexible substrate:** first, for ease of handling during the fabrication process, devices are fabricated on rigid substrate. Since the process is conducted on a rigid substrate, the device can be fabricated using various techniques such as high-temperature doping, oxidation, and lithography. **(2) Bonding flexible material:** to remove the rigid substrate and maintain the flexibility of the device, a flexible substrate such as PI is bonded onto the completed device fabricated on the SOI wafer [261, 262, 278]. In the process of bonding the SOI wafer and the flexible substrate, the buffer layer serves a crucial role in the aspect of structural defects. The buffer layer prevents cracks in the t-$SiO_2$ layers caused by Young's modulus difference during the Si etching process [277]. Generally, materials with Young's modulus in the GPa range similar to t-$SiO_2$, such as PI, are used to prevent these cracks [279, 280]. Subsequently, to bond the flexible substrate and the completed device on a rigid substrate, an adhesive material like silicone adhesive (Kwik-Sil) or depositing an additional bonding layer onto the buffer layer is utilized [261, 281]. Before bonding, the oxide layers are deposited on both sides of the flexible material. The oxide layers are used for bonding, and this bonding occurs by a strong covalent bond between the Si–OH of the oxide layer and the bonding layer. The covalent bonding occurs through strong bonds between atoms, forming Si–O–Si [282, 283]. To increase the number of Si–OH for bonding, a UV/ozone treatment is applied to the surface of the oxide layer [284, 285]. **(3) Etchi Si:** the rigid Si substrate is etched using the DRIE method. Specifically, using sulfur hexafluoride ($SF_6$) gas, F atoms in plasma state react with Si to form $SiF_4$, which facilitates the etching process ($SF_6 \rightarrow SF_4 + 2F; Si + 4F \rightarrow SiF_4$) [286]. In the Si etching process, the uniformity of the Si surface plays a crucial role in achieving precise etching of Si. Therefore, the CMP process, which is used in fabrication to smooth and planarize the surface of the wafer, is applied to polish the back surface of the SOI wafer. This process is aimed at the mirror-like surface of the substrate before the DRIE process, ensuring uniform etching depth, and reducing the heat applied to the sample during the process by decreasing the process time [277]. At this time, due to the selective etching properties between Si and $SiO_2$, the $SiO_2$ layer in the SOI wafer serves as an etch-stop layer [287, 288]. However, in the case of using t-$SiO_2$ encapsulation for the device, the t-$SiO_2$ layer can be damaged by the DRIE process after the complete etching of the Si substrate. Therefore, the precise etching time is important in the substrate removal process (figure 5(e)).

To ensure a long lifespan and stable device operation for the pH sensor, single-crystalline Si field-effect transistors (FETs) encapsulated with t-$SiO_2$ were achieved through substrate removal etching [261]. To assess the condition of patients with chronic diseases, there is a need for sensors that can continuously and accurately monitor bio signals in real-time within a liquid environment over an extended period without performance degradation [289]. This research has demonstrated the potential for a foundational waterproof and scalable biochemical sensor by creating a device with active electronics that exhibits excellent stability and pH detection performance. To enhance bio-fluid barrier properties, t-$SiO_2$ grown at 1000 °C was utilized on single-crystalline SiNMs as an encapsulation layer. The FETs were completely fabricated on the SOI wafer with a partial doping process. Before bonding the rigid substrate with the flexible substrate, PI was used as a buffer layer to prevent cracks in the t-$SiO_2$ layer caused by the significant Young's modulus difference between the bonding layer and the t-$SiO_2$ layer. Subsequently, using inductively coupled plasma reactive ion etching (ICP-RIE), the handling Si on the backside was removed to expose t-$SiO_2$ (figure 5(f)). Despite the submicron size of the device, this device exhibited minimal hysteresis (∼1 mV) due to its stable structure. Acceleration tests in PBS were conducted at 75 °C, 80 °C, 90 °C, and 100 °C, and the results matched the Arrhenius equation, demonstrating excellent encapsulation with reaction rates of ∼0.05 $nm{\cdot}d^{-1}$ at 25 °C and ∼0.26 $nm{\cdot}d^{-1}$ at 37 °C. These devices demonstrated consistent transistor performance even after multiple rounds of bending tests. Additionally, it was observed that the transistor's performance remained stable even after applying a static 1 V bias through the liquid gate (figure 5(g)). This device measures the response of transistors to standard pH buffer solutions utilizing an aluminum oxide ($Al_2O_3$) sensing layer functionalized on the Si gate electrode. An increased pH induces deprotonation of hydroxyl groups on $Al_2O_3$, resulting in an elevated negative charge, which causes a change in surface potential and shifts $V_{th}$ toward the positive direction. Presented as a function of extracted $V_{th}$ and pH values, this device demonstrates a sensitivity of (58.5 ± 3.9) $mV{\cdot}pH^{-1}$ (figure 5(h)). Consequently, utilizing the substrate removal etching process, flexible pH sensors were successfully encapsulated with t-$SiO_2$ on single-crystalline Si FETs, ensuring a long lifespan and stable device operation in biofluid environments.

Another study utilizing t-$SiO_2$ encapsulation on active Si MOSFET arrays involved the development of a long-lived, flexible, high-resolution active neural interface (figure 5(i)) [262]. To densely measure wide areas of the brain simultaneously, it is necessary to increase the throughput of the interface [290]. To achieve this, the researchers expanded the device to a kilo-scale setup to maintain a high electrode sampling density and reach a high number of channels. Passive devices have the disadvantage of requiring one wire per channel, making it challenging to achieve high resolution. To address this challenge, this research involved creating high-density electrodes with a large number of 28 × 36 channels active Si MOSFET arrays (figure 5(j)). The number of wires was significantly reduced by employing an active array, allowing for high-resolution measurements [144, 291–293]. Also, the interface production focused on the biocompatibility, lifespan, and device optimization for neural interfaces. To extend the lifespan within the body, the t-$SiO_2$ encapsulation strategy was employed on both the top and

bottom of the device. For t-$SiO_2$ encapsulation, devices were first fabricated on SOI, and a flexible layer was formed by spin-coating PI. Subsequently, a Ti/$SiO_2$ layer with a thickness of 1 $\mu$m was formed on PI using electron beam evaporation to facilitate bonding with a PI sheet containing another 1 $\mu$m layer of t-$SiO_2$. As a result, the two layers were bonded using UV-ozone-treated PDMS as an adhesive through OH bonding, which is a strong bond formed by the combination of OH groups on the PDMS surface and the $SiO_2$ surface [294]. Then rigid Si substrate was removed using ICP-RIE to produce flexible electronics. These electrodes were tested in both rodents and nonhuman primates (NHPs). Subsequently, when implanted into NHPs to record motor-related signals, the temporal changes in directional information from the central region of the primary motor cortex to the primary sensory cortex were observed when examining the spatiotemporal map (figure 5(k)). Then measuring the leakage current with the entire device implanted, all samples, except for the R1 sample, maintained a leakage current below 1 $\mu$A. Based on a dissolution rate of 0.46 nm·$d^{-1}$ for the 1 $\mu$m $SiO_2$ layer, the estimated lifespan of the device is approximately 6 years. Consequently, active Si arrays are successfully fabricated and capable of stable neural signal measurement in NHPs for over a year.

## 3. Bottom-up approaches

### *3.1. Chemical vapor deposition (CVD)*

CVD is a method of depositing a thin film onto the substrate surface through a chemical reaction by supplying a gas or powder containing the elements of the film. CVD is categorized as a bottom-up process because it involves depositing a nano-scale film, starting with individual atoms. CVD techniques, including plasma-enhanced CVD (PECVD) [295, 296], atmospheric pressure CVD [297], catalytic CVD [298, 299], and high-density plasma CVD [300] can be classified based on factors such as activation energy, reaction temperature, chamber pressure, and more. Si thin films, used in semiconducting electronics, can be deposited using CVD. However, conventional CVD methods require high temperatures to vaporize the source material. Consequently, applying Si thin films directly onto a flexible substrate becomes challenging. To overcome this limitation, fabrication methods have been developed to either reduce the process temperature for direct deposition on the substrate or create a flexible Si membrane without the need for direct deposition on the substrate.

*3.1.1. PECVD.* PECVD is commonly used for its ability to deposit or dope Si at lower temperatures. PECVD is a technique for creating a-Si or nano/microcrystalline Si thin films by generating plasma within a chamber [301–303]. When the reactive gas is introduced and a high voltage is applied vertically, the gas transforms into a plasma state. These ionized gases react chemically with each other, depositing the desired material on the substrate and releasing the remaining ions in a gas form. For example, when $SiH_4$ gas is injected into the chamber and a decomposition reaction occurs on the substrate due to plasma energy ($SiH_4 \rightarrow Si + 2H_2$). In this reaction, hydrogen ($H_2$) gas is exhausted, and Si is deposited on the substrate [115, 304]. In PECVD, the low-temperature process is possible due to plasma energy (<250 °C). The reason why the low-temperature processes are achievable is that PECVD utilizes high-energy plasma instead of high-temperature heat energy, thereby reducing the activation energy required for the source material activation. The necessity for a low-temperature process arises from the fact that flexible substrates, used in flexible electronics, primarily consist of organic materials vulnerable to heat. Therefore, to directly deposit Si on the substrate, the process temperature has to be sufficiently low for the substrate to endure. Recent research aims to reduce the process temperature to expand the range of flexible substrates that can be utilized [115, 174, 175, 305]. Additionally, PECVD allows Si doping at low temperatures. Conventional doping methods of Si are categorized into two types: thermal diffusion and ion implantation, both necessitating high-temperature processes. In thermal diffusion, Si is heated to around 1000 °C, enabling the doping material to diffuse into the Si crystal [185–188]. On the other hand, ion implantation involves a high-temperature annealing process to recrystallize the damaged lattice resulting from the energy imparted during ion implantation [306–308]. In contrast, Si doping with PECVD can be achieved through the process of injecting a doping precursor gas without a high-temperature process. The doped Si layer can be deposited by injecting a mixture of precursor gases such as diborane ($B_2H_6$), phosphine ($PH_3$) (used for doping), and silane ($SiH_4$) (used for Si deposition) at an appropriate ratio, or an intrinsic Si layer is deposited followed by the injection of gases used for doping to achieve partial doping (figure 6(a)) [51, 309].

a-Si:H thin films deposited using PECVD are widely used to fabricate flexible solar cells. The a-Si exhibits a greater light absorption coefficient compared to single-crystalline Si. The well-ordered structure of single-crystalline Si, with well-defined bond lengths and angles, minimizes internal light scattering. In contrast, amorphous and microcrystalline structures possess disturbing bond lengths and angles, leading to the light scattering increment. Therefore, a-Si solar cells efficiently absorb light due to this light scattering, which helps prevent unwanted light reflectance and achieves a light-trapping effect. Due to the high absorption coefficient of a-Si, a-Si requires less material, such as the absorption layer thickness, compared to crystalline Si [95]. Consequently, a-Si solar cells are suitable for flexible solar cells that demand thin Si for flexibility [95].

Flexible Si solar cells are fabricated by directly depositing a-Si on flexible substrates, such as PI and colorless polyimide (CPI), utilizing the low-temperature process of PECVD. There are two cases for improving performance: one involves applying a unique structure, and the other involves enhancing applicability by combining other functions. Three-dimensional (3D) hexagonal arrays of nanoholes were created through sol–gel chemistry and soft thermal NIL on the zinc oxide/PI substrate, and then p/i/n a-Si:H layers were directly deposited on the patterned PI substrate at under

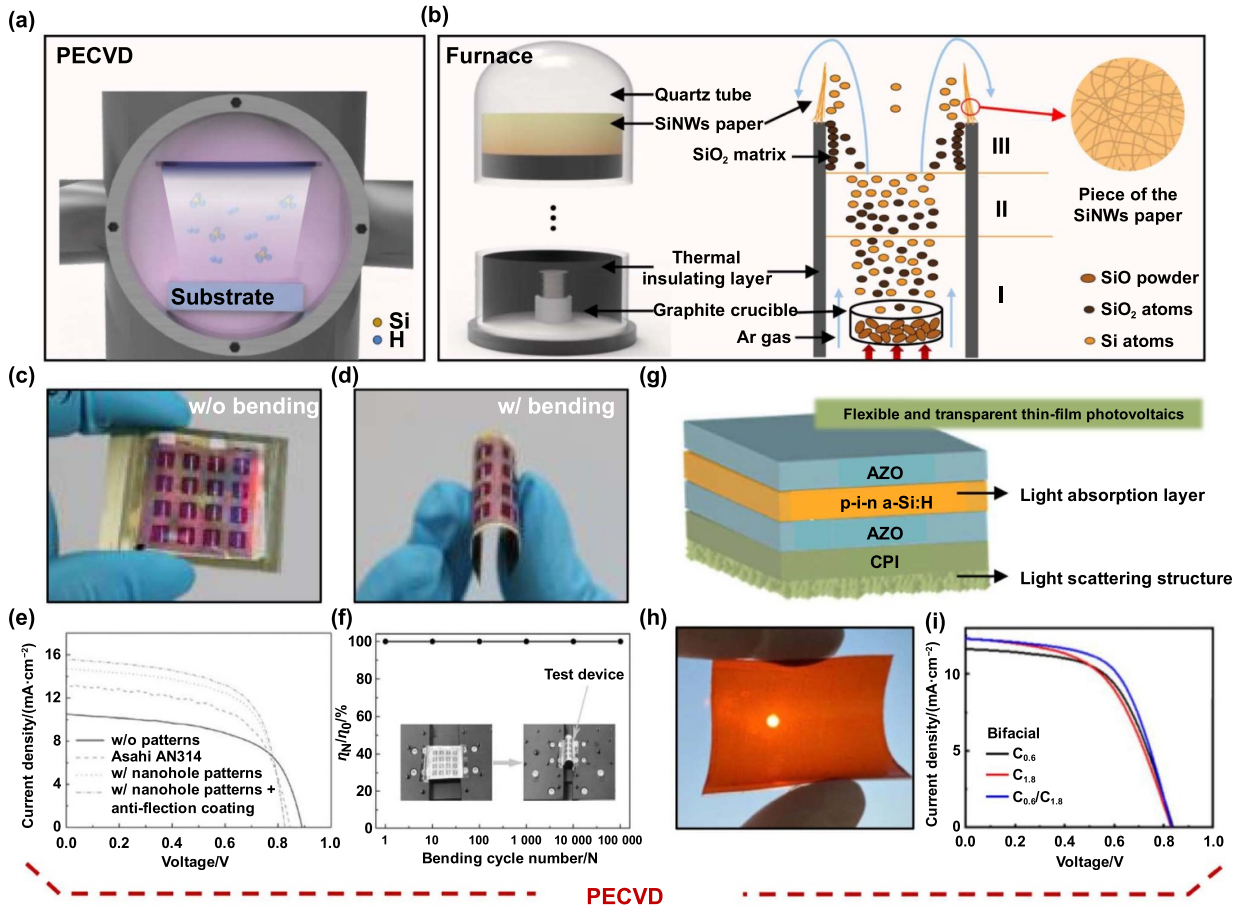


**Figure 6.** Chemical vapor deposition in bottom-up approach. (a) Si thin-film deposition through PECVD. (b) Silicon nanowire paper (SiNWP) deposition using furnace, employing SiO powder and a carrier gas. Reprinted with permission from [310]. Copyright (2013) American Chemical Society. (c) and (d) Photograph of flexible a-Si:H solar cells on patterned PI substrate without and with bending. (e) Current density-voltage curves of the solar cell according to substrate types; PI substrate with and without nanotextured patterns, Asahi AN314 (commercial textured FTO glass substrate), PI substrate with nanotextured patterns and anti-reflection coating. (f) Relative efficiency function of bending cycles (∼100 000). Inset: bended device installed in measuring equipment. [114] John Wiley & Sons. © 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (g) and (h) show flexible, transparent solar cell on a CPI substrate. (i) Bifacial current density-voltage characteristics of solar cell. Measurements on the front condition of 1 sun and back condition of 0.3 sun (power conversion efficiency = 6.15%). Reproduced from [115]. CC BY 4.0. (j) and (k) show the photograph and schematic of large-area and foldable Si solar cell. (l) Normalized power of 140 $\mu$m and 60 $\mu$m modules as a function of the incident angle of light. (m) Development of the device area of flexible c-Si solar cell. Reproduced from [175]. CC BY 4.0. (n) Optical image of SiNWP adhered to a PDMS substrate during bending. (o) Scanning electron microscope image of SiNWP. Inset shows the optical image of SiNWP on printed paper demonstrating transparency. (p) SERS spectra of thiram residues from the lemon peel surface with AuNP-SiNWP (upper) and AuNP-SiNWP torn off from the lemon (lower). Reprinted with permission from [311]. Copyright (2017) American Chemical Society.

250 °C (figures 6(c) and (d)). Applying the nanohole structure improved broadband-enhanced light absorption and power conversion efficiency. The efficiency of a-Si:H solar cell based on the textured PI film with an anti-reflection coating was 8.17%, while that based on the PI film without patterns was 5.5% (figure 6(e)). Additionally, due to the improved mechanical flexibility achieved by utilizing nanoholes, there was almost no drop in efficiency even after 100 000 bending cycles (figure 6(f)) [114]. In the other research, transparency was added to flexible solar cells by using the transparent CPI substrate (figure 6(g)). Flexible and transparent solar cells have the potential to be used in building-integrated photovoltaics (BIPV). BIPV is a technology that involves the installation of solar cells on the exterior walls and windows of buildings, eliminating the need for a separate installation site. This technology is gaining attention because this allows solar cells to be integrated into various exterior surfaces, enabling power generation even in buildings with limited available space and without compromising their aesthetics. This research fabricated a flexible and transparent solar cell incorporating a double n-type rear window layer integrated with a light scattering structure on a CPI substrate (figure 6(h)). CPI is widely used as the substrate in flexible and transparent solar cells due to its higher glass transition temperature compared to other polymers like polyethylene terephthalate and polycarbonate, as well as its high optical transparency [116]. A light scattering structure within CPI was utilized to enhance the performance of thin film solar cells. The cell was deposited on the opposite side of the light-scattering structure to utilize its light-scattering properties and minimize defects

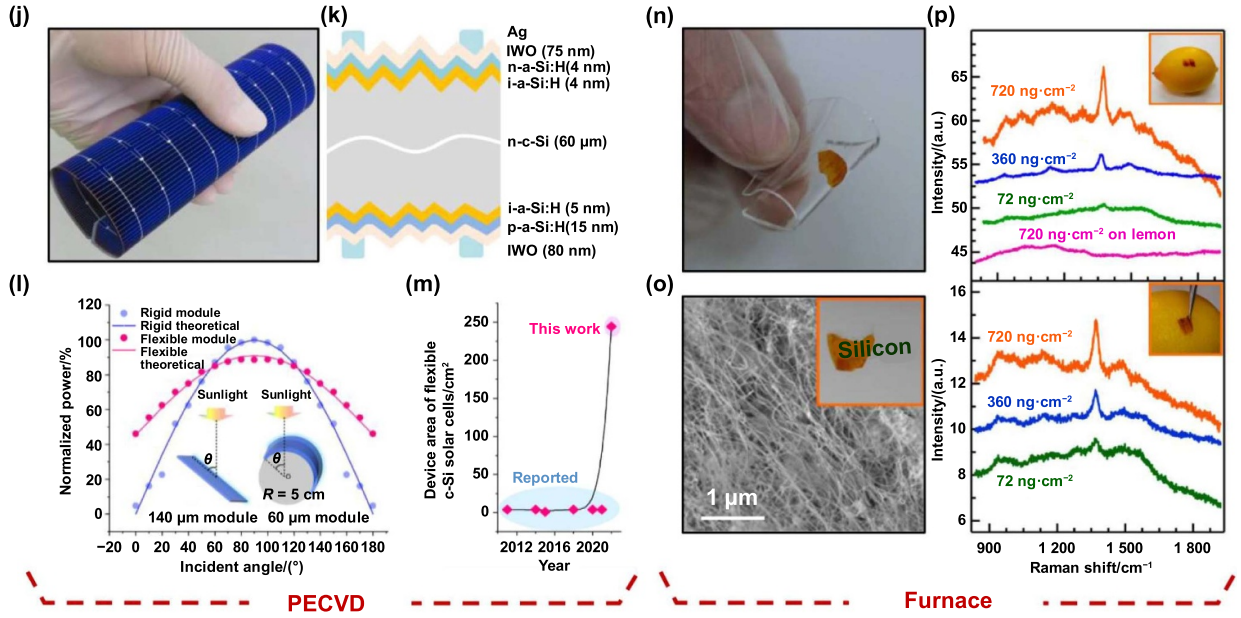


**Figure 6.** (Continued.)

in the cell caused by surface stress during the deposition of a-Si:H absorption layers. In this step, $p^-/i/n^-$ a-Si:H layers were deposited using PECVD at 250 °C. $SiH_4$ was used for depositing a-Si:H layer and $B_2H_6$, $PH_3$, and $CO_2$ gases were used for doping. A dual rear window layer was implemented to not only minimize optical losses but also enhance electron transport for rear-facing incident light, ultimately boosting performance in bifacial operation. In the case of bifacial operation, where 1 sun was irradiated on the front and 0.3 sun was irradiated on the back, the solar cell achieved a bifacial power conversion efficiency of 6.15%, demonstrating its exceptional performance (figure 6(i)). The bifacial operation can produce electricity using both front and rear incident light, enabling the efficient use of solar cells and making them suitable for BIPV [115].

When doping a-Si with PECVD, the doping type of a-Si can be adjusted depending on the precursor gases. Utilizing this doping process, this research fabricated a foldable Si heterojunction (SHJ) solar cell (figures 6(j) and (k)). Conventional bulk Si wafers are brittle and crack under bending because of their thick thickness. To improve flexibility, this research reduced the Si wafer thickness to 60 $\mu$m. However, this reduction in thickness decreased light-harvesting efficiency due to the indirect optical bandgap of Si. To compensate for the decreased efficiency, this research attempted to reduce the reflectance of incident light by chemically texturing microscale pyramids onto the surface. Nevertheless, when the bending force was applied to the textured wafer, the maximum stress was located in the sharp regions between the pyramid structures on the surface in the marginal region of the wafer, leading to the initiation of cracks in this region. To address this issue, the pyramid structures at the edge were blunted to improve flexibility. Subsequently, doped Si layers can be deposited using PECVD without a high-temperature doping process. a-Si:H layers were deposited at 200 °C, creating n/i/n/i/p a-Si:H heterojunction. SHJ solar cell consists of the n-type crystalline Si absorber with a stack of a-Si layers. Additionally, the p-doped a-Si:H layer formed the pn junction, while the n-doped a-Si:H layer also contributed to surface passivation. The graph showed the normalized power as a function of incident light angles for both a 140 $\mu$m rigid solar cell and a 60 $\mu$m flexible solar cell affixed to a 5 cm black cylinder. Notably, although the flexible module exhibited slightly lower power at normal incidence (90°), it remarkably outperformed the rigid module with a 17% increase in integrated power across incident angles ranging from 0° to 180° (figure 6(l)). Additionally, this progress led to significant enhancements in both device area and power conversion efficiency of flexible solar cells, increasing from 4 $cm^2$ and 23.27% to 244.3 $cm^2$ and 24.5%, respectively (figure 6(m)). Considering that 140 $\mu$m wafers constituted approximately 50% of the total device cost, the utilization of 60 $\mu$m wafers resulted in a substantial 29% reduction in production expenses. Consequently, a large-area and foldable Si solar cell was successfully developed while retaining the advantages of SHJ solar cells, such as high efficiency [175].

*3.1.2. Furnace.* Another CVD method involves creating a flexible SiNWs membrane using a furnace instead of depositing Si directly on the substrate (figure 6(b)). To prepare the SiNWs membrane, 99.99% pure silicon monoxide (SiO) powder within a graphite crucible is heated to about 1600 °C. During the heating process, SiO is in a metastable state and decomposes into $SiO_2$ and Si ($2SiO \rightarrow SiO_2 + Si$). Si and $SiO_2$ vapors are carried upward by the constant flow of Ar carrier gas and stratify due to the greater molecular weight of $SiO_2$ compared to Si (figure 6(b), part II). The process of

forming the SiNWs paper-like membrane can be divided into four steps: (1) $SiO_2$ vapor reaches the orifice of the graphite cylinder and deposits on the cylinder's upper surface, forming a $SiO_2$ matrix. Si vapor precipitates within this matrix. (2) SiNW nuclei form and continue to grow as Si vapor is continuously supplied through a constant gas flow. (3) The intensity of the carrier gas flow influences the direction of SiNW growth. As the carrier gas flows upward, SiNWs grow in the same direction and spontaneously interlock with each other. Finally, SiNWs membrane are created through the assembly of individual SiNWs (figure 6(b), part III). By cutting the SiNWs, a flexible and self-standing SiNWs paper-like membrane is produced. The furnace-based method eliminates the need for hazardous precursor gases like $SiH_4$ or $SiCl_4$, eliminating the need for a purification system and ensuring safe Si production. These properties also make this method cost-effective [310, 311].

Furnace-fabricated silicon nanowire paper (SiNWP) is well-suited for applications requiring flexibility, transparency, and cost-effectiveness. Surface-enhanced Raman scattering (SERS) generates an electromagnetic amplification effect through localized surface plasmons, enabling the detection and identification of molecules at low concentrations. Noble metal nanostructures, such as Au and Ag, are predominantly used as SERS substrates due to their ability to focus nanoscale light from plasmon resonance. Hence, to enhance SERS performance and enable the application to various materials, the SERS platform has to be flexible, transparent, and possess a noble metal nanostructure. In this research, flexible SiNWP was applied to the SERS platform to conform to surfaces with random curvature and expand the surface area for analyte adsorption, facilitating *in situ* detection of toxicants on food surfaces. Additionally, the transparency of the platform can address the opacity issue hindering direct analysis of adsorbed analytes (figure 6(n)) [312]. The SiNWP comprised high-density nanowires forming a three-dimensional porous network structure, providing transparency and flexibility (figure 6(o)). Additionally, SiNWs, with their high refractive index, can be strongly polarized under light excitation, acting as subwavelength dielectric antennas to trap light and enhance the localized field. Consequently, SiNWP exhibited strong optical field enhancement and good SERS activity. Combining plasmonic gold nanoparticles (AuNPs) with SiNWP improved SERS performance while preserving the flexibility and transparency of the pristine SiNWP. Pesticide residues were detected by affixing a small piece of Au NP-SiNWP to the lemon surface sprayed with pesticide residues. The SERS spectra of thiram residues were obtained through two schemes (figure 6(p)). In the upper part of figure 6(p), the SERS spectra of thiram residue obtained from the lemon peel surface with SiNWP are shown. For thiram molecules, the Raman spectrum closely resembled that of lemon. By introducing AuNP-SiNWP, the Raman signal for thiram was enhanced, enabling low-dose detection. In the lower part of figure 6(p), SERS spectra, measured by transferring AuNP-SiNWP torn off from the lemon surface to a flat Si substrate or glass before complete ethanol evaporation are shown. This method can also detect concentrations as low as 72 $ng{\cdot}cm^{-2}$. As AuNP-SiNWP was applied to the SERS platform for detecting food inspection, the transparency of SiNWP allowed the incident laser and Raman scattering signals to easily pass through AuNP-SiNWP and the flexibility of SiNWP allowed for conformal contact on curved food surfaces, enabling low-dose detection [311].

### 3.2. Physical vapor deposition (PVD)

PVD is a method that involves depositing a thin film by vaporizing a source material using physical force without a chemical reaction. PVD can be categorized into three primary techniques: thermal evaporation [313], e-beam evaporation [314], and sputtering [315], depending on the type of energy used to vaporize the target material. In the case of the e-beam evaporator, materials with high melting points such as Si can be used as a source due to the high energy of the e-beam. Therefore, thin Si films can be deposited using an e-beam evaporator. Additionally, in contrast to thermal evaporation, which heats the crucible with source materials using resistive heating, the e-beam evaporator minimizes the contamination risk because the source materials are directly heated without the crucible [314]. The e-beam evaporation operates as follows: when high voltage is applied to the filament, the filament heats up and emits electrons. Subsequently, these emitted electrons are guided to the crucible through the induced magnetic field. Upon reaching the crucible, the incident electrons collide with the source material, releasing heat energy. As a result, this heat energy vaporizes the source material, and then the vaporized source material deposits onto the substrate (figure 7(a)) [316, 317].

Si is the promising next-generation lithium-ion-batteries (LIBs) anode with a high theoretical capacity of about 4200 $mAh{\cdot}g^{-1}$. However, Si anode faces two major challenges. **(1) Large volume expansion:** when lithiated with $Li_xSi$, the volume of Si expands by approximately 300%. This repeated expansion and contraction during charging and discharging lead to Si pulverization, resulting in a rapid decrease in energy capacity and shortened battery life. **(2) Excessive solid electrolyte interphase (SEI) layer formation:** the SEI layer is formed on the surface of the anode material when reacting with the lithium (Li) ions. Although the SEI layer has low electronic conductivity, the SEI layer exhibits high Li ion conductivity and acts as a pathway for Li ions between the electrolyte and the anode material. However, during the expansion and contraction of Si, the SEI layer on the Si surface tends to break into several small pieces, allowing for repeated interaction between Si and Li ions through the gaps created. This continuous lithiation of Si particles leads to Li consumption and gas generation, resulting in the thickening and hardening of the SEI layer. This limits the oxidation-reduction reaction of Li, reducing energy capacity

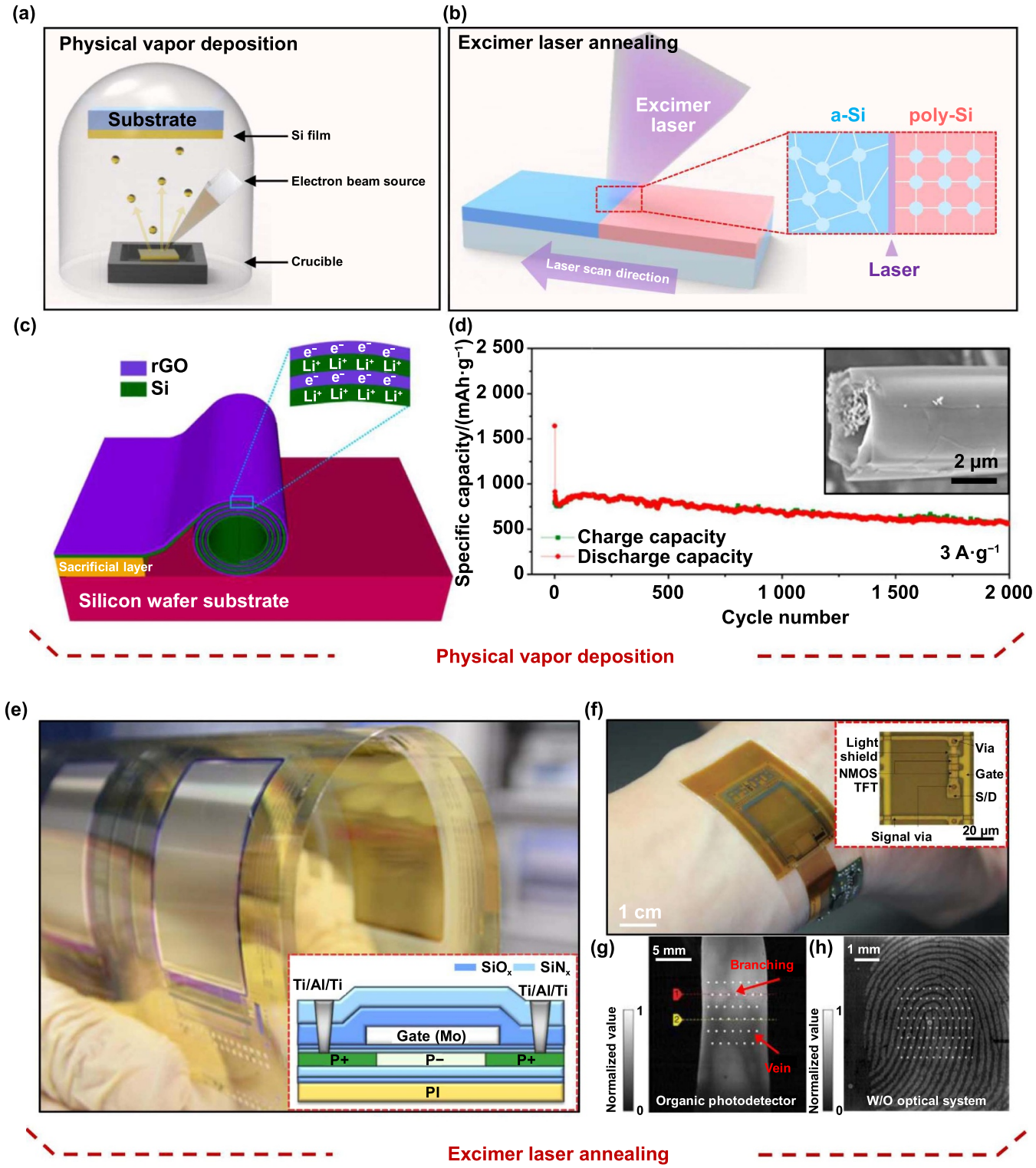


**Figure 7.** PVD and excimer laser annealing in bottom-up approach. (a) Fabrication using PVD. The illustration depicts the E-beam evaporator. (b) a-Si can be converted into poly-Si through excimer laser annealing, with a-Si deposited using diverse methods. (c) Schematic illustration of flexible lithium-ion batteries comprised of Si/rGO bilayer anodes. Silicon is generated using E-beam evaporator. (d) Cycling performance at 3 $A \cdot g^{-1}$. Reprinted with permission from [176]. Copyright (2015) American Chemical Society. (e) Photograph of a flexible poly-Si thin-film transistor. Poly-Si is generated through laser annealing. Reprinted with permission from [106]. Copyright (2017) American Chemical Society. (f) Photograph of a conformable imager attached to an arm. This imager incorporates poly-Si TFTs and a NIR organic photodiode. (g) Finger vein image captured by conformable imagers. White dots are added to protect personal information. (h) Fingerprint image captured by a conformable imager without an optical system. Reproduced from [107], with permission from Springer Nature.

and shortening battery life. These challenges hinder the practical use of Si anode materials [318, 319]. These issues can be alleviated by designing appropriate nanostructures or adding protective coatings to Si. Moreover, transforming 2D structures into 3D structures, such as spiral and roll-up, can create additional internal space for electron and ion transport while accommodating volume changes during lithiation/delithiation [320]. Therefore, this article represents a sandwich nanoarchitecture structure consisting of Si/reduced graphene oxide (rGO) bilayer nanomembranes to create a Si anode (figure 7(c)). Si nanofilm served as the electrochemically active layer for Li storage and rGO functioned as a flexible conductive protecting layer. The photoresist was spin-coated onto a Si wafer substrate, which served as a sacrificial layer. Subsequently, the a-Si nanofilm was deposited on the sacrificial layer using an e-beam evaporator, where the amorphous structure of a-Si promoted lithiation and accommodated the first cycle of strain. Finally, rGO was spin-coated onto the Si film, functioning as a flexible protecting layer. This rGO layer enhanced cycling performance by accommodating volume changes and preventing aggregation of Si nanoparticles. These nanomembranes were naturally rolled up into cylindrical shapes due to the built-in strain released by selective etching of the sacrificial layer. This unique property allowed for their use as flexible LIBs. The capacity graph shows 3 $A{\cdot}g^{-1}$ at 2000 cycles with only minimal degradation of 3.3% per 100 cycles (figure 7(d)) [176]. The Si/rGO nanoarchitecture functioning as anodes in LIBs demonstrated an extended cycling life and good capacity retention.

### 3.3. Excimer laser annealing & AIC

Methods for crystallizing a-Si into poly-Si include excimer laser crystallization [321], metal-induced crystallization [322, 323], and solid-phase crystallization [324, 325]. Unlike a-Si, poly-Si has a more ordered atomic structure, facilitating electron movement and resulting in significantly higher electron mobility. Increased electron mobility enhances the performance of poly-Si thin-film transistors (TFTs) by improving power and data transmission [52]. However, to apply poly-Si to flexible electronics, the process has to be conducted at a low temperature to accommodate the use of a flexible substrate. Therefore, we introduce two methods that employ low-temperature a-Si crystallization for flexible electronics: excimer laser annealing and AIC.

*3.3.1. Excimer laser annealing.* Excimer laser annealing is used as a low-temperature process for crystallizing a-Si. The high absorption of a-Si prevents the ultraviolet light from penetrating the substrate, preventing the substrate from heating. This characteristic enables a low-temperature process, making it permittable for heat-vulnerable substrates and enabling the fabrication of flexible electronics using poly-Si [326–328].

Excimer laser annealing process is as follows: initially, a-Si was deposited using PECVD, followed by furnace annealing at under 350 °C for dehydrogenation. The furnace annealing must be carried out at a temperature that the substrate can withstand [329]. When the excimer laser with high energy density is irradiated to the a-Si layer, a-Si absorbs this high energy. This absorption is possible because a-Si has a high absorption coefficient [95]. When the absorbed energy exceeds the energy of breaking the bonds between the a-Si atoms, the bonds are broken and Si rapidly melts. Following this, the molten Si quickly solidifies. During the rapid solidification, Si atoms arrange themselves into a crystalline structure. After completing the laser annealing step, these crystal grains grow and merge to create a poly-Si structure (figure 7(b)) [330–332].

LTPS, obtained through excimer laser annealing, can be applied to TFTs. Compared to a-Si, organic, and metal-oxide TFTs, LTPS TFTs exhibit high electron mobility and fast switching speeds due to their crystalline structure. By implementing LTPS TFTs on a flexible substrate, they can be used as flexible TFTs themselves or integrated with other devices requiring TFTs. In this research, p-channel LTPS TFT was fabricated on a flexible PI substrate. The channel poly-Si was crystallized with a 308 nm XeCl excimer laser and then lightly doped with boron. For the formation of $p^+$ in the source/drain regions, the regions were self-aligned by boron implantation (figure 7(e)) [106].

Developing high-speed, high-resolution flexible imagers is crucial for obtaining high-quality vital signs. The flexible imagers can contact conformally with the skin, allowing for obtaining distinct biometric authentication (e.g. vein and fingerprint) and the continuous monitoring of vital signs. Also, high-mobility TFTs are necessary to accelerate switching speeds, enabling faster image data capture and readout. In this research, flexible imagers were fabricated by combining LTPS TFTs capable of reading small photocurrents ($<$10 pA) with low noise and organic photodetectors with high light detection sensitivity in the near-infrared region (figure 7(f)). LTPS TFTs played a key role in achieving high speed and resolution. Also, due to its low-temperature process, LTPS TFTs can be applied to flexible electronics. The mobility was 40 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ and the readout time of data was reduced to 60 $\mu$s. Moreover, the on/off ratio was high at $10^7$, allowing the integrated device to rapidly read out low-intensity near-infrared light signals. This imager offered a resolution of 508 pixels per inch and a speed of 41 frames per second. Furthermore, biometric signals, such as fingerprint and vein images, can be obtained and used to map pulse waves. The finger vein image, taken by the conformable imager, captured essential vein authentication data, such as vein branch point, branching angle, and vein counts (figure 7(g)). The fingerprint image was captured without an optical system. This image contained precise authentication details including the number of ridges, the branch point, the endpoint, and sweat gland locations. In other words, this imager can achieve a clear

fingerprint image without the need for optical lenses, making it possible to capture fingerprints even in a dark environment (figure 7(h)). This conformable imager can simultaneously acquire biometric information and measure biosignals. Moreover, its conformability to any part of the body enables continuous, high-precision, and stress-free health monitoring [107].

*3.3.2. Aluminum-induced crystallization (AIC).* Metal-induced crystallization involves crystallizing a-Si to poly-Si at a low temperature. We introduce a method for fabricating poly-Si thin film using aluminum (Al). AIC can be processed below 400 °C because Al significantly reduces the activation energy required for crystallization [333].

This method can be explained in three steps. **(1) Deposition of Al and a-Si:** Al (bottom)/a-Si (top) layer is deposited through sputter both to the same thickness on a flexible substrate. At this step, the Al layer is utilized to enable low-temperature crystallization. Originally, high temperatures were required for the crystallization of Si due to the necessity of breaking the strong covalent bonds of Si. However, this method allows for a low-temperature process by reducing the activation energy required for crystallization through the Al layer. The free electrons at the metal layer adjacent to a-Si cause a screening effect, which weakens the covalent bonds of the a-Si layer at the interface between the metal and Si layer. Because of this bond weakening, the activation energy for the diffusion of Si atoms adjacent to the interface is lower than that of bulk Si atoms. In other words, Si atoms at the interface can diffuse along the interface even with low activation energy, enabling crystallization nucleation to occur at a lower temperature [333]. **(2) Annealing a-Si:** annealing is performed in a nitrogen environment at 400 °C for 1 h, crystallizing a-Si into poly-Si. This transformation occurs through the interaction between the Al and a-Si layers. During the annealing, Si atoms first dissolve into the Al layer and then diffuse within it. Consequently, Si nuclei initiate the formation at the grain boundary of Al crystals. These nuclei grow in all directions within the Al layer until they make contact with adjacent grains, thus establishing a poly-Si film on the substrate. In this step, layer exchange occurs for the following reasons: the continuous diffusion and crystallization of Si atoms, occurring within the Al grain boundaries, create free space in the original a-Si layer and accumulate compressive stress in the Al grains. These two effects suggest that Al tends to occupy the free space in the Si layer to relieve stress. As a result, the Si layer formed at the original Al layer location due to the growth of Si grains, displacing the original Al layer. Al moved to the original a-Si layer location, causing a layer exchange. **(3) Al removal and obtain poly-Si film:** the poly-Si thin film is obtained by removing the top Al layer with Al etchant. AIC allows the achievement of large-grained poly-Si film with excellent electrical properties (figure 8(a)) [177, 178].

Through the AIC process, poly-Si can be utilized in flexible electronics at low temperatures. Applying poly-Si to flexible temperature and pressure sensors enables the creation of sensors with higher sensitivity compared to those made with a-Si. Therefore, this research focused on fabricating a sensor using poly-Si. While there are various methods for measuring pressure, they chose the piezoresistive type of sensor due to its suitability for easy signal processing and its ability to prevent crosstalk between sensing signals when measuring multiple parameters. The poly-Si resistor on the outer side of the sensor functioned as a temperature sensor, while the one on the inner side served as both a pressure and temperature sensor. Placing the poly-Si piezoresistor at the edge of the circular membrane received the highest strain, thereby increasing pressure sensitivity. The inner poly-Si resistor can sense both pressure and temperature changes, allowing it to obtain the absolute pressure signal $(\Delta R = \mathrm{GF}\cdot\varepsilon\cdot R;\ R = \mathrm{Resistance},\ \varepsilon = \mathrm{Strain})$ by subtracting the resistance changes on the outside $(\Delta R_{\mathrm{outside}} = \mathrm{TCR}\cdot\Delta T\cdot R;\ T = \mathrm{Temperature})$ from those on the inside $(\Delta R_{\mathrm{inside}} = (\mathrm{GF}\cdot\varepsilon + \mathrm{TCR}\cdot\Delta T)\cdot R)$. The pressure sensor had a sensitivity of 1.01 $\mathrm{mV\cdot kPa^{-1}}$ with a resolution of 100 Pa, while the temperature sensor had a sensitivity of 2.26 $\mathrm{mV\cdot{}^{\circ}C^{-1}}$ with a resolution of 0.1 °C. Choosing PI as a substrate served two purposes: providing flexibility and matching the thermal expansion coefficient with poly-Si to prevent stress mismatch during the annealing (figure 8(b)). Due to the flexibility and the ability to monitor both pressure and temperature, this technology can be applied to applications in electronic skin and brain-implantable devices (figure 8(c)) [179].

### 3.4. Vapor–liquid–solid (VLS)

The VLS method is a process that uses a metal droplet as a catalyst to accumulate Si underneath the droplet through precursor gas, primarily employing gases like $SiCl_4$ to grow Si structure. To facilitate forming droplets of metal catalyst at a low temperature, the low eutectic point of the metal and substrate is required. The metal catalyst to form a liquid droplet in a liquid state acts as a trap of the growth materials. The VLS is often widely utilized for creating SiNWs because it enables the anisotropic formation of structures [336–338]. Since these SiNWs only deposit and grow within the metal catalyst area during their formation, the SiNWs are grown toward the anisotropic direction. The diameter and position of the SiNWs are determined by the metal catalyst size and position [339]. The VLS method not only has relatively cost efficiency but also produce Si with high crystal quality at a low-temperature process compared to CVD [335, 339].

This process involves three main fabrication processes. **(1) Deposit metal layer on Si:** the VLS method is growing Si structure using a metal catalyst. Typically, in the VLS method of SiNWs growth, the Au is used as the metal catalyst [340]. This choice is related to the eutectic point of Au–Si, which occurs at a relatively low temperature of 363 °C [341]. Therefore, at above 363 °C, Au–Si alloy droplets in a liquid state are formed on the surface of the Si substrate [342, 343]. Au is thinly deposited on the Si substrate to serve as the catalyst for Si growth by using sputter or thermal evaporation. **(2)**

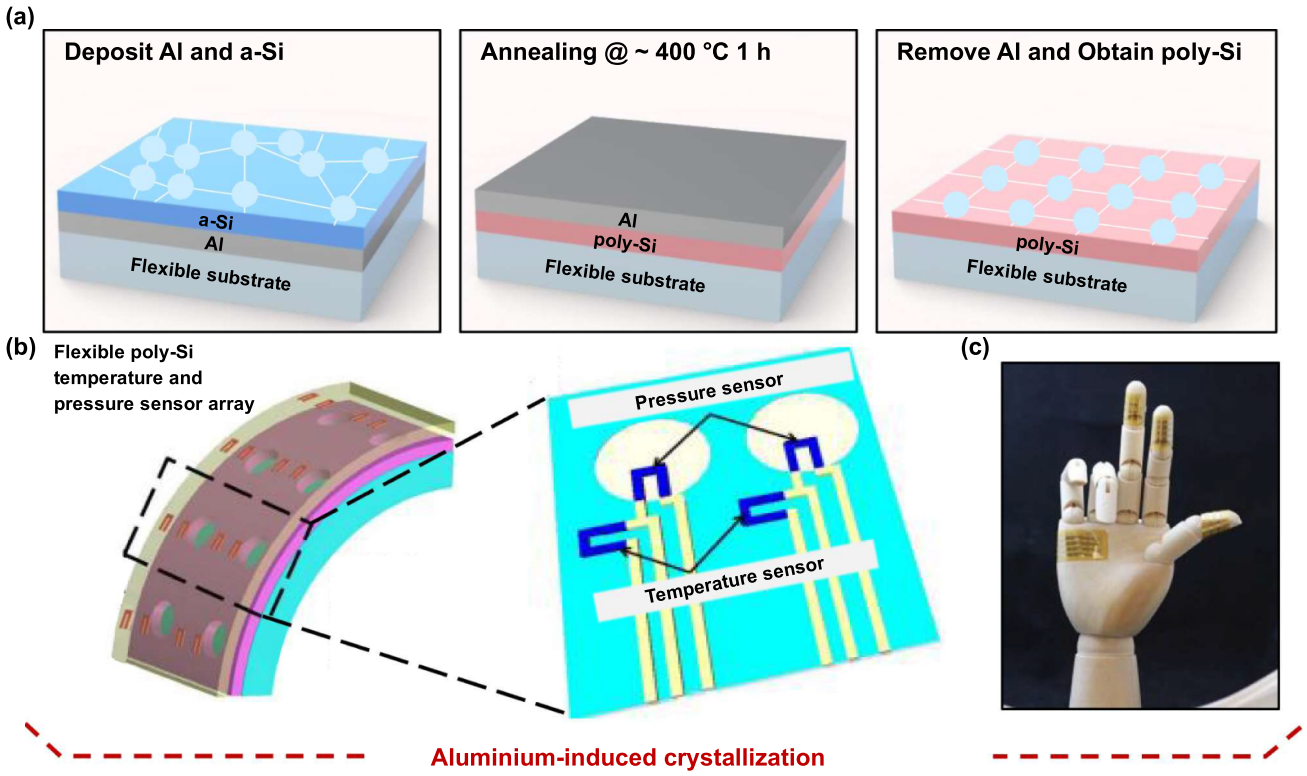


**Figure 8.** Aluminum-induced crystallization and vapor–liquid–solid. (a) Fabrication process using aluminum-induced crystallization. (b) Schematic illustration of flexible poly-Si temperature and pressure sensor array. All sensors are based on poly-Si resistors. (c) Photograph of the entire device detached to a mannequin hand. © [2017] IEEE. Reprinted, with permission, from [179]. (d) Fabrication process using vapor–liquid–solid. (e) Optical images of the flexible transistor array devices. (f) Schematic structure of biosensing platform based on SiNW-FET device. (g) Output characteristics of the transistors with a 6 $\mu$m interelectrode (IE) spacing. [334] John Wiley & Sons. © 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (h) SEM image of radial tandem p–i–n junction solar cell (RTJ) solar cell. (i) Schematic structure of RTJ solar cell. (j) Current–voltage characteristics of RTJ solar cell as a function of bending radius. Reprinted from [335], © 2021 Elsevier Ltd. All rights reserved.

**Dewet metal layer:** to form the Au–Si droplets, annealing the Si substrate surface with high temperature is conducted. To facilitate droplet formation for VLS growth, the metal catalyst needs to be capable of forming a liquid alloy with the substrate materials. To control the size and location of SiNWs, the size and location of the droplets need to be controlled. First, the size of the droplets is determined by the thickness of the deposited Au layer. According to the increase in the thickness of the metal catalyst layer, the size of the formed droplets is increased by the thermal annealing process. Then, to control the location of the droplets, an etched hole pattern is formed on the additional t-$SiO_2$ layer on the surface of the Si. Subsequently, only a certain position of Si is exposed to the surface. As a result, the location of the droplets can be adjusted by condensing the metal only on the exposed Si position through the annealing process after the metal catalyst deposition [344]. These approaches allow for the controlled formation of Si wires with specific diameters and positions. **(3) Grow c-SiNWs:** $SiCl_4$ vapor is absorbed on the surface of the catalyst droplets, initiating chemical reactions at the interfaces. Subsequently, the growth materials diffuse into the liquid phase and begin to saturate the droplets. When the droplets reach a supersaturation state, Si deposits onto the substrate in solid form, leading to crystal growth and the formation of the SiNWs structure $(SiCl_4 + 2H_2 \rightarrow Si + 4HCl)$ [345]. During the SiNWs growth process, the solubility of the metal catalyst needs to be low to minimize crystal defects of SiNWs. The commonly used Au, with its low solubility $2 \times 10^{-4}$ at% in Si at a high temperature of 1280 °C, is well suited as a metal catalyst. To apply the SiNWs for flexible electronics, transferring SiNWs onto a PI foil and growing SiNWs on a metal foil substrate is used [334, 335].

The VLS method was utilized to fabricate the flexible SiNW-FETs for biomedical diagnostic devices [334]. A key challenge in biomedical diagnostic devices is to reduce the cost of the device and make it lightweight in a cost-effective manner [346–348]. The VLS method enabled the creation of a lightweight and flexible diagnostic platform using SiNW-FET technology, which exhibits a low detection limit for the DNA sequence of influenza A subtype H1N1 while maintaining high detection accuracy [334]. The SiNW-FET shows high output current and lower power loss for high gain and power efficiency [349]. In this research, VLS was utilized for the fabrication of SiNWs with a diameter of 22 nm on rigid Si, ranging in length from 3 $\mu$m to 20 $\mu$m. SiNWs were transferred to a 100 $\mu$m thick PI for flexible device design. For the transfer to PI, a contact printing method was applied. In this approach, the SiNWs arrayed on the donor Si wafer were attached using

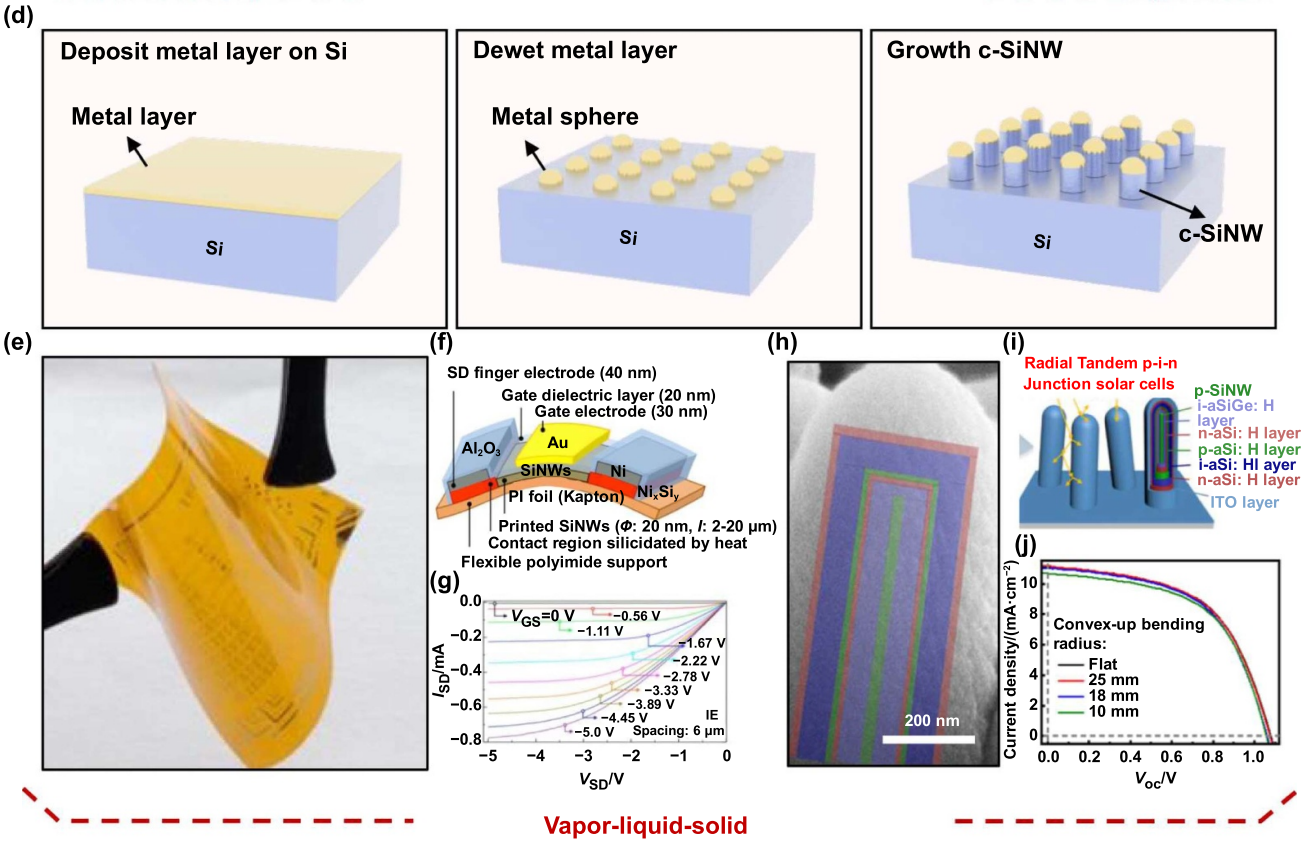


**Figure 8.** (Continued.)

a metal sledge. The sledge followed a pre-defined path, and through van der Waals interactions, it enabled the separation of SiNWs onto the flexible substrate. Subsequently, the nanowires were aligned horizontally on the PI to construct the FET. This polymer-based device is nearly 10 times lighter than the thick Si, which can be as much as 500 $\mu$m thick. A single nanowire provides an output current of 1 $\mu$A, so a parallel array is applied to increase current output and operational range [350–354]. The source and drain electrodes were deposited using nickel, and the passivation layer which used $Al_2O_3$ was deposited with the gate Au electrode (figures 8(e) and (f)). The maximum saturation source-drain current up to 1 mA is achieved at $-5$ V source-drain voltage and $-5$ V source-gate voltage, with a subthreshold swing of 130 mV per dec$^{-1}$ (figure 8(g)). The device achieved low power loss and mechanical stability using SiNWs. Consequently, the SiNW-FET-based biomedical diagnostic device demonstrated a high analytical performance with a very high detection limit.

The SiNW-based flexible solar cell was fabricated using the VLS method. High power-to-weight ratio (PTWR) is a crucial performance index for high-performance flexible/portable solar cells. A high PTWR provides significant advantages for future power sources like small drones and airships, allowing for increased power output per unit weight [355]. To enhance the power of solar cells, an advanced tandem solar cell structure needs to be applied for the broad light absorption spectrum. Traditional a-Si:H thin film solar cells have a wide bandgap of up to 1.75 eV, resulting in light absorption limited to $\lambda < 700$ nm. To extend this spectrum, the solar cell needs to have two p/i/n junctions with wider/narrower bandgaps, resulting in a tandem solar cell structure. Conventional planar tandem solar cells have a-Si:H/microcrystalline silicon ($\mu$c-Si:H). However, the $\mu$c-Si:H layer is typically thick, around 2 $\mu$m, which limits flexibility [356–358]. To address this issue, SiNWs grown utilizing the VLS method have reduced the need for such thick bottom layers. Additionally, SiNWs enhance light absorption efficiency by separating the optical absorption path from the electrical separation distance. The SiNWs are grown on an Al foil substrate with a thickness of 15 $\mu$m using the VLS method with Sn as a catalyst and demonstrate a tandem multilayer structure composed of p-type Si nanowire/intrinsic a-SiGe:H/n-type a-Si:H/p-type a-Si:H/intrinsic a-Si:H/n-type a-Si:H/indium tin oxide using a plasma-assisted technique (figures 8(h) and (i)). This SiNW-based solar cell exhibits excellent flexibility, with only a slight efficiency drop of 3.9% even when bent with a 10 mm bending radius (figure 8(j)). Furthermore, it significantly increases the light absorption spectrum and demonstrates outstanding PTWR performance. Consequently, this tandem solar cell composed of SiNWs demonstrates high performance and flexibility.

## 4. Conclusion

Si, with its remarkable properties, stands as a prominent material across diverse fields. The emergence of various fabrication methods for utilizing Si in flexible electronics has enabled its application in more diverse fields compared to rigid devices while retaining its inherent properties. This review introduces the fabrication approaches employed in flexible Si electronics.

However, each method has its inherent limitations. Despite efforts to develop new approaches to overcome these issues, the integration of Si into flexible electronics poses several challenges, including performance degradation, complex processing steps, and sensitivity to temperature and chemical treatments. Therefore, researchers must explore various methods to address these essential problems.

These are the directions for development we propose: developing a process that allows for the utilization of Si without performance degradation and complex processing steps is needed. Advancements in transferring Si onto flexible substrates and enhancing the durability of flexible substrates would facilitate superior device fabrication in the top-down approach. Additionally, advancing methods for depositing Si on flexible substrates also ensures the maintenance of the Si performance in a bottom-up approach. Furthermore, the implementation of 2.5D and 3D Si architecture significantly contributes to miniaturization, thereby expanding functionality in Si-based flexible electronics. These advancements would significantly amplify the potential of Si, enabling its full exploitation in emerging technologies and applications.

Continuous efforts are being made to realize flexible Si fabrication and its diverse applications through both top-down and bottom-up approaches. This holds the promise of continuous breakthroughs that are prepared to shape the future of various industries, particularly within flexible electronics.

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